TI 6490.20

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INSTRUCTION BOOK

# M200
# MATRIX PRINTER

## (GENERAL DESCRIPTION, THEORY, AND TROUBLESHOOTING)

PART OF

## FLIGHT SERVICE AUTOMATION SYSTEM

VOLUME IV



CONTRACT DTFA01-81-C-10039



CONTRACTOR

E-SYSTEMS, INC.
GARLAND DIVISION
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FEDERAL AVIATION ADMINISTRATION

TI 6490.20

MASTER SUPPORT
AND LOGISTICS MANUAL

VOLUME I OF II

# M-SERIES MATRIX PRINTERS

GENERAL DESCRIPTION

THEORY OF OPERATION

TROUBLESHOOTING




*Dataproducts*

6200 CANOGA AVENUE
WOODLAND HILLS, CALIFORNIA 91365

APRIL, 1983

## SPECIAL NOTE TO READER

Despite every reasonable effort by Dataproducts Corporation, a manual of this scope may contain errors, omissions, or ambiguities. To a large extent, we depend upon feedback from our users to correct this situation. We urge you, therefore, to let us know how you think this manual can be improved. The best way to do this is to use the Reader's Comment Sheet located at the back of the manual.

Dataproducts Corporation grants the Federal Aviation Administration specific limited rights as provided for in General Provision 42. Rights In Technical Data and Computer Software, paragraph B., entitled "Governments Rights." These limited rights (including the right to duplicate) are applicable to all Maintenance and Operation Manuals for the Dataproducts B series equipment provided under this Contract DTFA01-81-C-10039. Use of this data is specifically for the FSAS project only.

**WARNING:** This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with instruction manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subjart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

1. Reorient the receiving antenna.
2. Move the printer away from the receiver.
3. Plug the receiver into a different outlet so that printer and receiver are on different branch circuits.
4. Consult an experienced radio/TV technician for additional suggestions.

**CAUTION**

To avoid the possibility of a shock hazard, fire, or violation to your equipment warranty, any INTERNAL modifications of your equipment should be done ONLY by a qualified service representative.

**NOTE**

Do to connector pin impedances, an unshielded plug or cable may cause radiation interference. The printer is designed for use with an adequately shielded interface cable. The shield must be bonded directly to the chassis of the printer.

## SPARE PARTS ORDERING INFORMATION

Parts can be ordered as follows:

For orders placed by telephone, call the appropriate number as shown below:

If customer facility is located east of the Mississippi River:

(213) 887-8033

If customer facility is located west of the Mississippi River:

(213) 888-4091

For orders placed via Telex, use:

67-4473 DATAPROD LSA

For orders placed via mail, address to:

DATAPRODUCTS CORPORATION
21300 Roscoe Boulevard
Canoga Park, CA 91304

Attention: Order Administration

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Dataproducts Corporation provides comprehensive repair services for all product lines.

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Circuit card and subassemblies are tested and repaired utilizing components and assembly/test procedures which meet or exceed original product specification.

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THE M-SERIES INSTRUCTOR TRAINING GUIDE: The Instructor Training Guide provides all necessary information to accurately conduct a training course on Dataproducts M-Series Matrix Printers. The guide provides the instructor with overall course strategy, detailed theory of operation, lecture preparatory notes, laboratory directions and sample problems, exams, exam answer sheets, and viewgraph slide masters.

THE M-SERIES STUDENT TRAINING GUIDE: Used by the student in conjunction with the training course, this text provides pictorial aids which simplify concepts.

THE M-SERIES SLIDE/CASSETTE TRAINING PROGRAM: This Slide/Cassette Program delivers a sound module-level understanding of the M-Series printers, enabling the trainee to perform all required maintenance, calibrations and adjustments, disassembly and reassembly, and to troubleshoot and resolve printer problems in a logical and orderly way. Lecture and laboratory are presented via photographic slides and tape cassettes. Each program includes an M-Series Maintenance Guide and a slide/cassette Student Guide.

FOR REGISTRATION OR ORDERING INFORMATION, CALL:

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TECHNICAL EDUCATION CENTER

(213) 887-8489

Telex: 67-4473

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# SECTION I

# GENERAL DESCRIPTION

## 1.1 INTRODUCTION

This Master Support and Logistics Manual describes the Dataproducts Corporation's M-Series (M120/M200) matrix printers. Volume I consists of the following sections:

Section I - General Description

Section II - Theory of Operation

Section III - Troubleshooting

Volume II consists of the following sections:

Section IV - Schematic and Logic Diagrams

Section V - Illustrated Parts Lists

## 1.2 SUPPORTING DOCUMENTS

Two additional documents complement this Master Support and Logistics Manual:

a. M120/M200 User's Guide, Publication No. DPC255174.

b. M120/M200 Maintenance Guide, Publication No. DPC255074.

## 1.3 PURPOSE OF EQUIPMENT

The M-Series is a family of microprocessor-controlled matrix printers designed for use as output peripherals for minicomputer terminals and small business systems. Data is supplied by the user in either parallel or serial form, and printed bidirectionally. Characters are formed in a 7 x 7 dot matrix. The dots are produced by print wires striking an inked ribbon against the paper form.

## 1.4 DIFFERENCES BETWEEN MODELS

Two models of the M-Series printer family are described in this manual:

a. Model M120 Medium Speed Serial Matrix Printer.

b. Model M200 High Speed Serial Matrix Printer.

The principal difference between the two models is the print rate. The Model M120 printer prints at a nominal rate of 75 lines per minute for 132 printed character columns, while the Model M200 print rate is 125 lines per minute for 132 printed character columns. The M120 printer uses a single-column print head of seven print wires; the M200 printer uses a dual-column print head of seven print wires each, for a total of 14 print wires. Other differences include hardware circuits that drive the print wires, shuttle servo motor, and firmware routines involved in printing.

Throughout this manual, the paragraph, figure, and table headings that apply uniquely to either the M120 or M200 printer are designated by the applicable model number. Headings not designated by a specific model number apply to both models.

## 1.5 FEATURES

### 1.5.1 Standard Features

Following is a list of M120/M200 standard features:

a. Front Forms Load
b. Bottom Forms Load
c. Horizontal Alignment Guide
d. Vertical Alignment Guide
e. Easy Loading Ribbon Cassette
f. Paper Out Sensor
g. Condensed Printing
h. Expanded Printing
i. High Speed Paper Slew
j. Forms Thickness Control
k. Status Display
l. Built-In Self Test
m. 6 Lines Per Inch Print Lines

### 1.5.2 Optional Features

The M120/M200 options are described in paragraph 1.12.

## 1.6 PHYSICAL DESCRIPTION (Figures 1-1 through 1-4)

The printer is made up of seven major physical components, as follows:

a. Print Head
b. Shuttle System
c. Ribbon System
d. Paper Feed System
e. Power Supply
f. Control Panel
g. Circuit Card Assemblies

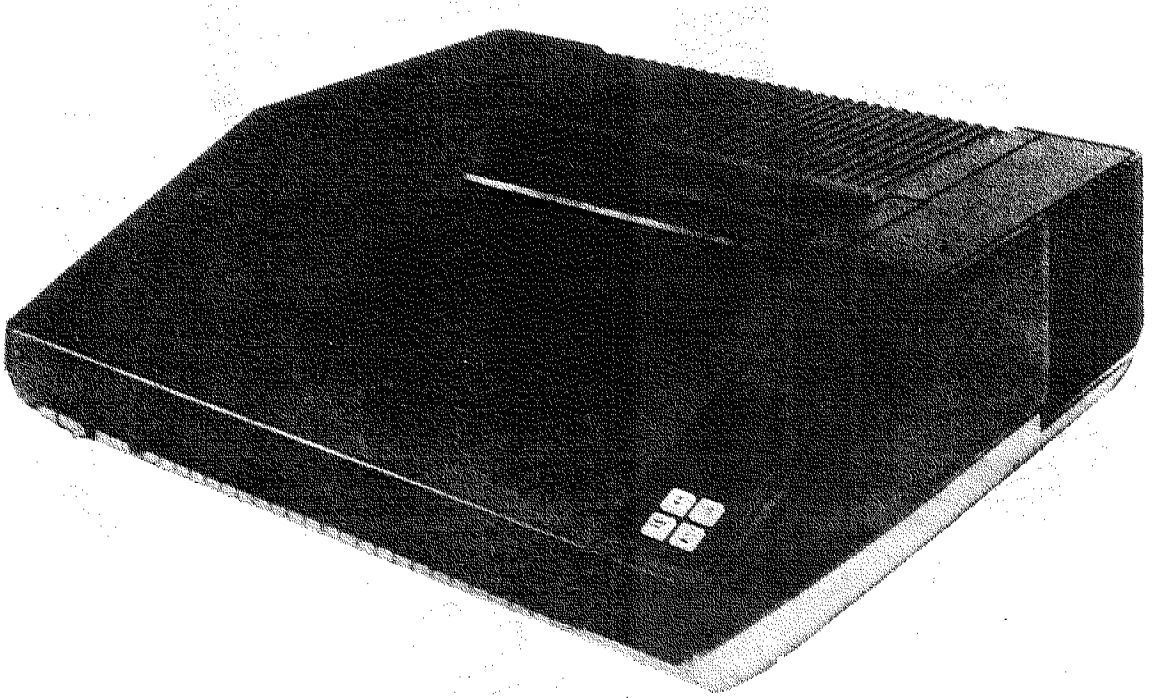

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Figure 1-1. M-Series Printer

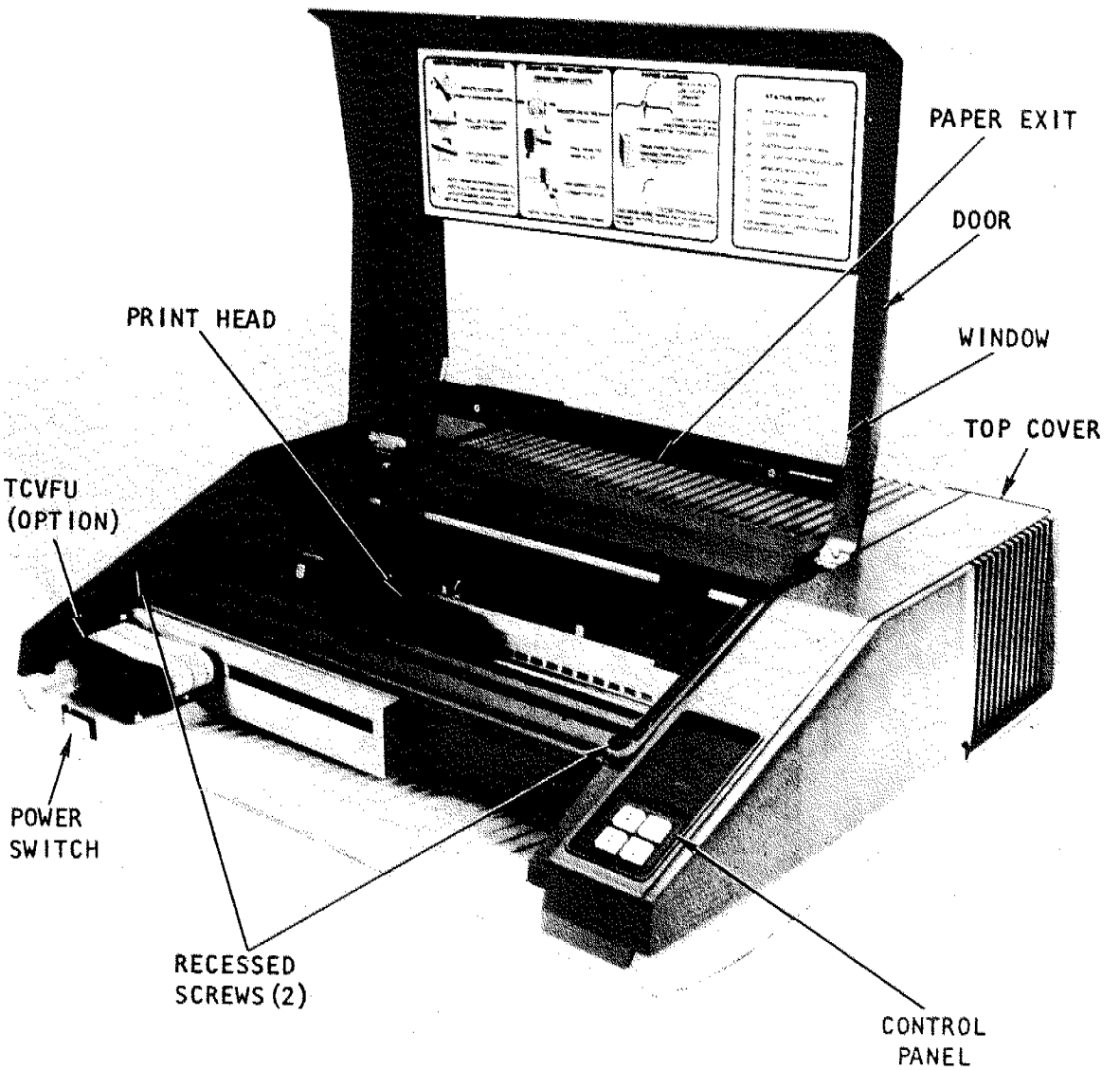



Figure 1-2. Printer, 3/4 View, Window Raised

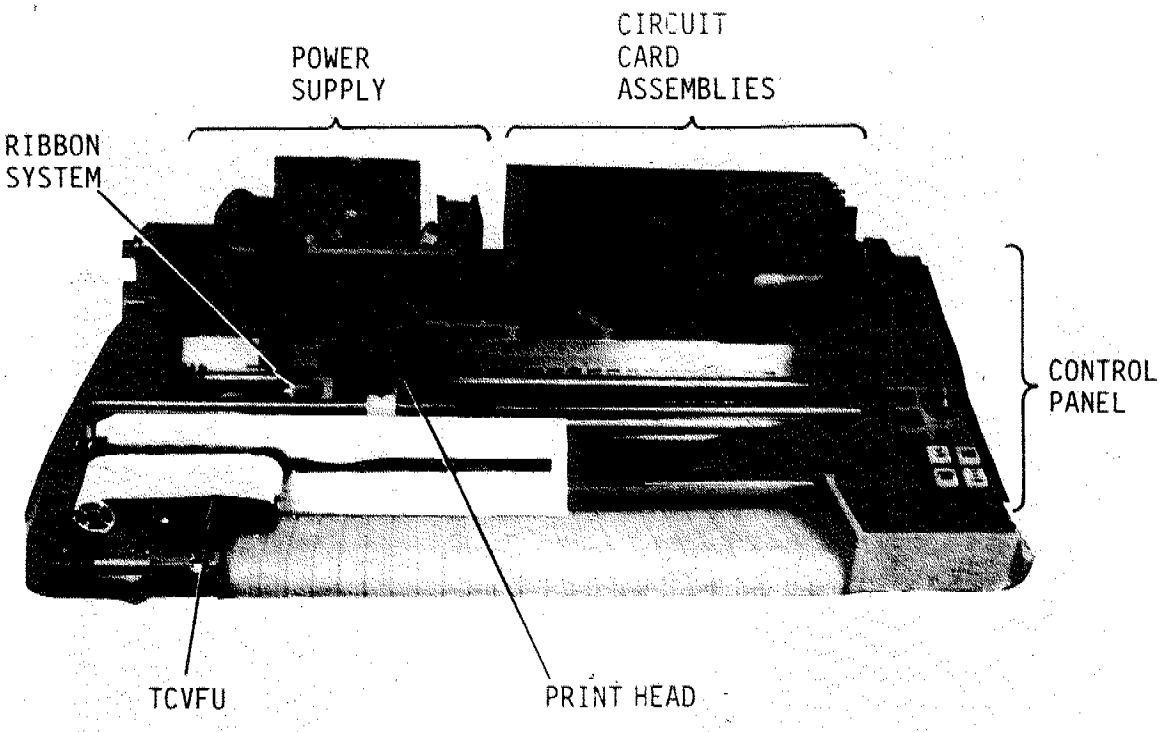



Figure 1-3. Printer Front View, Cover Removed

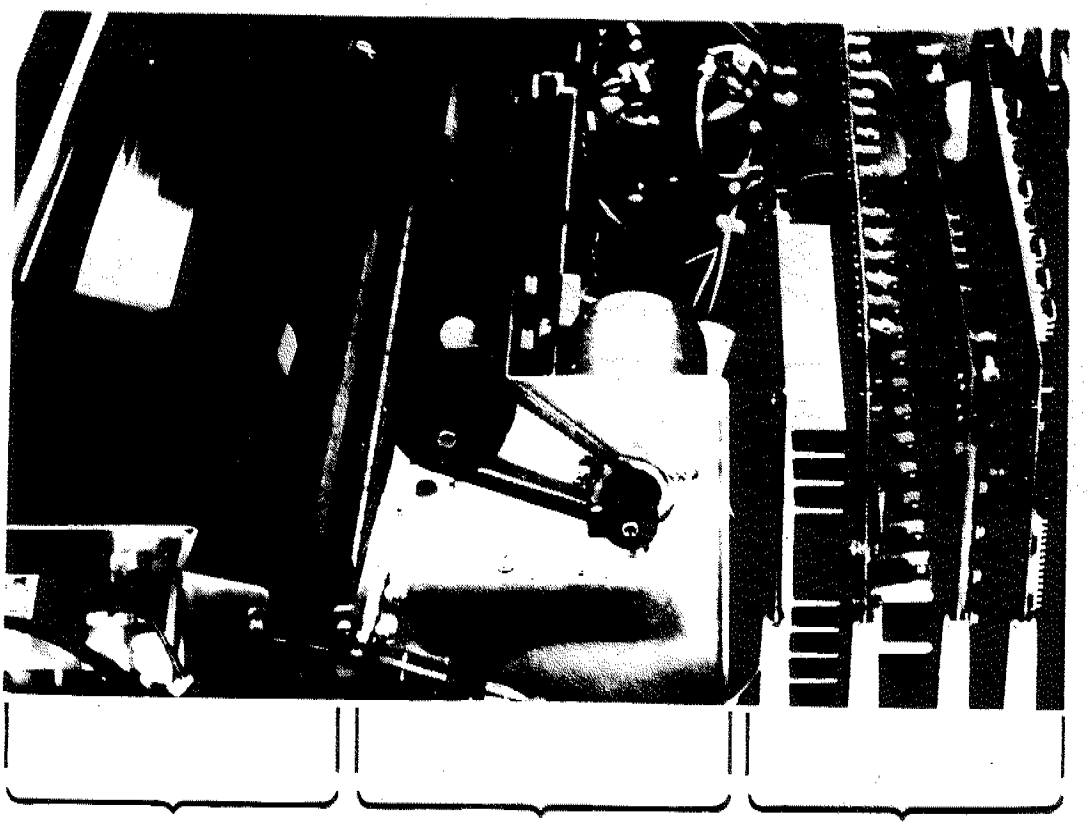



Figure 1-4. Printer Top Right View, Cover Removed

These components are enclosed in a clamshell plastic package, and mounted on the bottom half of the package. The two halves of the clamshell package are locked at the back by two quick-release latches, and secured at the front by two recessed screws. To gain access to all components of the printer, the top portion of the clamshell package, the top cover, is removed. The control panel is located under the top cover, and fastened by a spring-loaded clip. When removing the top cover, the control panel is detached and placed in a recessed area within the printer chassis. A hinged portion of the top cover, the door, is raised, as shown in figure 1-2, to gain access to the print head and ribbon cassette. A plastic window within the door allows a view of the line currently being printed while the door is closed. Paper exits at the top through a slot within the top cover.

## 1.7 M200 PRINT HEAD

The M200 printer uses a 14-wire head to produce dot pattern characters (matrix). The fourteen print wires are arranged in two vertical columns of seven wires each. Figure 1-5 illustrates the dot configuration of the character "M" within the matrix.

## 1.8 M120 PRINT HEAD

The M120 printer uses a seven-wire, single-column print head to produce the dot pattern characters. In all other respects, the printing principles of the M120 are identical to those of the M200. Figure 1-6 illustrates the dot configuration of the character "M" in the M120 printer.

## 1.9 PRINTER ASSEMBLY ORGANIZATION AND DESCRIPTION

The printer assemblies and their interconnections are illustrated in figure 1-7. With the exception of the Tape Controlled Vertical Format Unit (TCVFU) option, all assemblies are interconnected either directly or by cable via the Mother Board Circuit Card Assembly (A7). The TCVFU interfaces with the printer via the Interface Circuit Card Assembly (A2).

Circuit card assemblies A2 through A6 are interconnected with the printer via P1 and P2 on the Mother Board Circuit Card Assembly (CCA). All other assemblies are connected with the Mother Board CCA by plug and jack, as shown in figure 1-7. The J14 (PA) and J15 (PB) shown in figure 1-7 are allocated for option configuration switches described in section VI of the M120/M200 User's Guide, DPC 255174.

The following assemblies are described in subsequent paragraphs:

a. Power Supply Components and Regulator Circuit Card Assembly
b. Interface Circuit Card Assembly
c. Processor Circuit Card Assembly
d. Motor Driver Circuit Card Assembly
e. Wire Driver Circuit Card Assembly
f. Print Head and Shuttle Mechanism
g. Ribbon Advance Components
h. Paper Feed Components
i. Control Panel

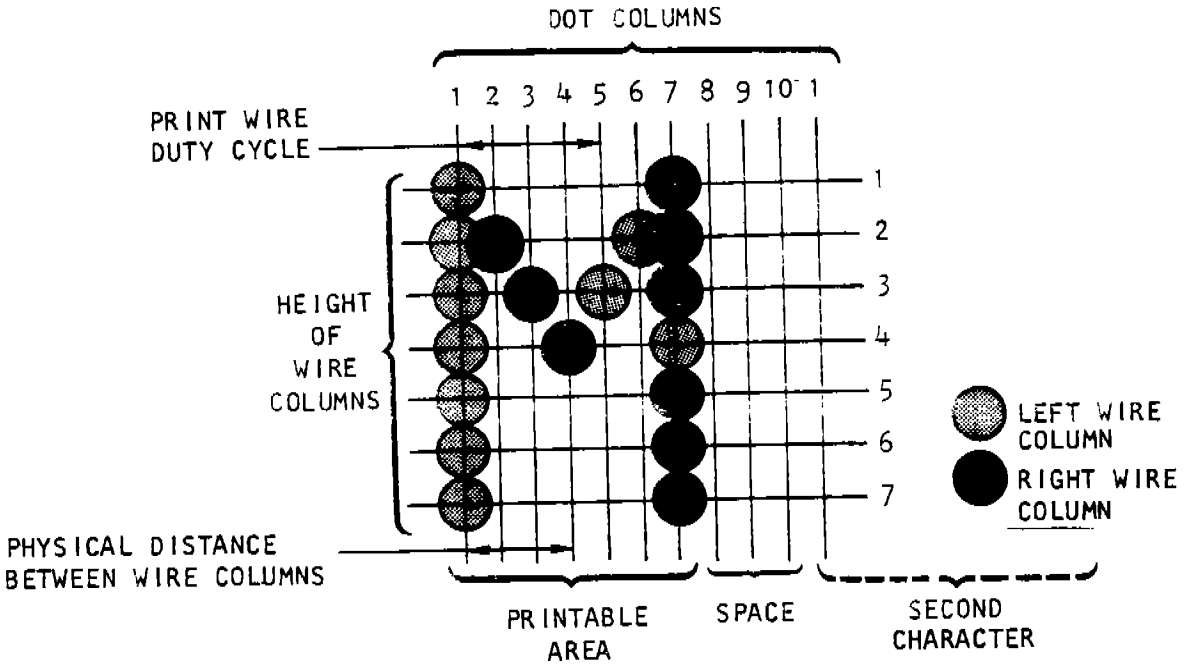



Figure 1-5. M200 Character Matrix and Formation

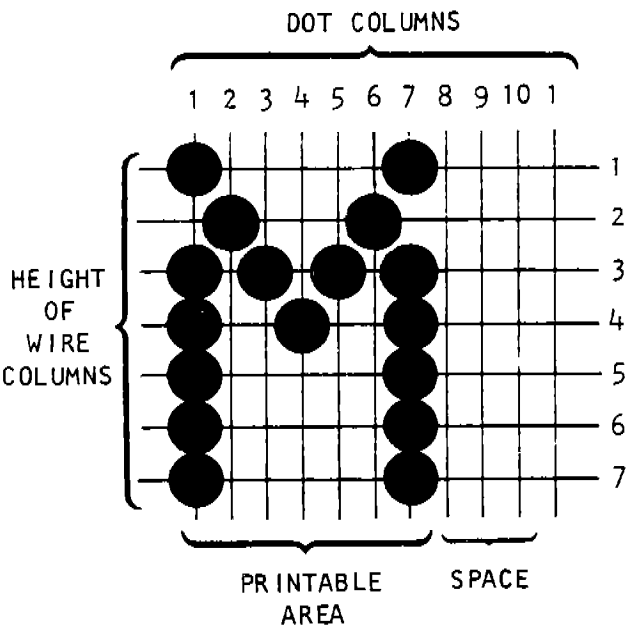



Figure 1-6. M120 Character Matrix and Formation

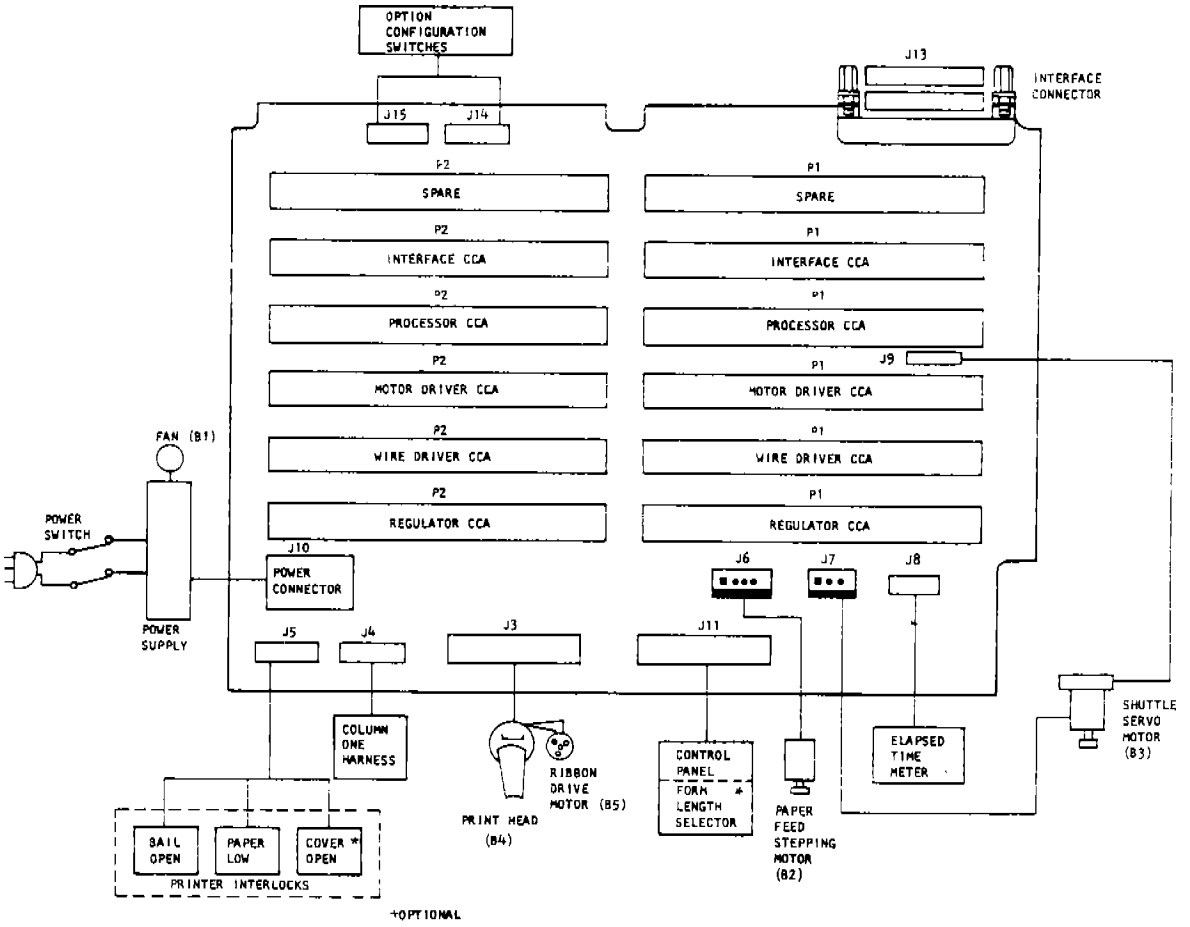



Figure 1-7. Printer Assembly Interconnection Diagram

### 1.9.1 Power Supply Components

The printer is configured with a universal power supply. As such, it can accept either domestic or international line power in any one of four different voltage/frequency combinations, as follows:

a. 115 VAC (nominal) at 60 Hz

b. 230 VAC (nominal) at 60 Hz

c. 115 VAC (nominal) at 50 Hz

d. 230 VAC (nominal) at 50 Hz

As shown in figure 1-8, the main component of the universal power supply is universal transformer T1. A primary winding of T1 forms a resonant circuit with resonant capacitor C4 at the incoming line frequency, driving the transformer core into saturation. As a result, T1 produces constant secondary voltages over a wide range of primary line voltage variations.

Other components of the power supply include fuses, main power switch, thermostat, line filter, bridge rectifiers, and filter capacitors.

Three filtered DC output voltages are produced by the power supply: +9V, +21V, and -21V. These output voltages are used either directly throughout the printer, or applied to the Regulator CCA for further regulation.

The Regulator CCA (A6) receives filtered inputs of $\pm$21 VDC and +9 VDC, and outputs regulated $\pm$12 VDC, +9 VDC and an adjustable +5 VDC (see section III). The regulated voltage outputs from the Regulator CCA are placed on the P1 and P2 buses of the Mother Board CCA and distributed throughout the printer.

### 1.9.2 Interface Circuit Card Assembly (A2)

The primary function of the Interface CCA is to interface the user system with the printer. Interface requirements differ among the various user systems with which the printer can operate. For this reason, the printer may be configured with the standard Interface CCA described in this section, or with one of the following optional Interface CCAs: DPC Parallel Long Line Interface CCA, DPC Centronics-Compatible Interface CCA, or Serial Interface CCA. Optional interface signals are described in section II of this manual and in section IV of the M120/M200 User's Guide, DPC 255174.

The standard Interface CCA (A2) is a short-line interface circuit card assembly which operates at a maximum cable length of 49 feet (15 meters). It is recommended that the interface cable be constructed of 22 AWG insulated wire. Each signal in the cable should be transmitted over a twisted wire pair, with one of the wires serving as a return. Voltage levels for signals transmitted over this interface are defined as follows:

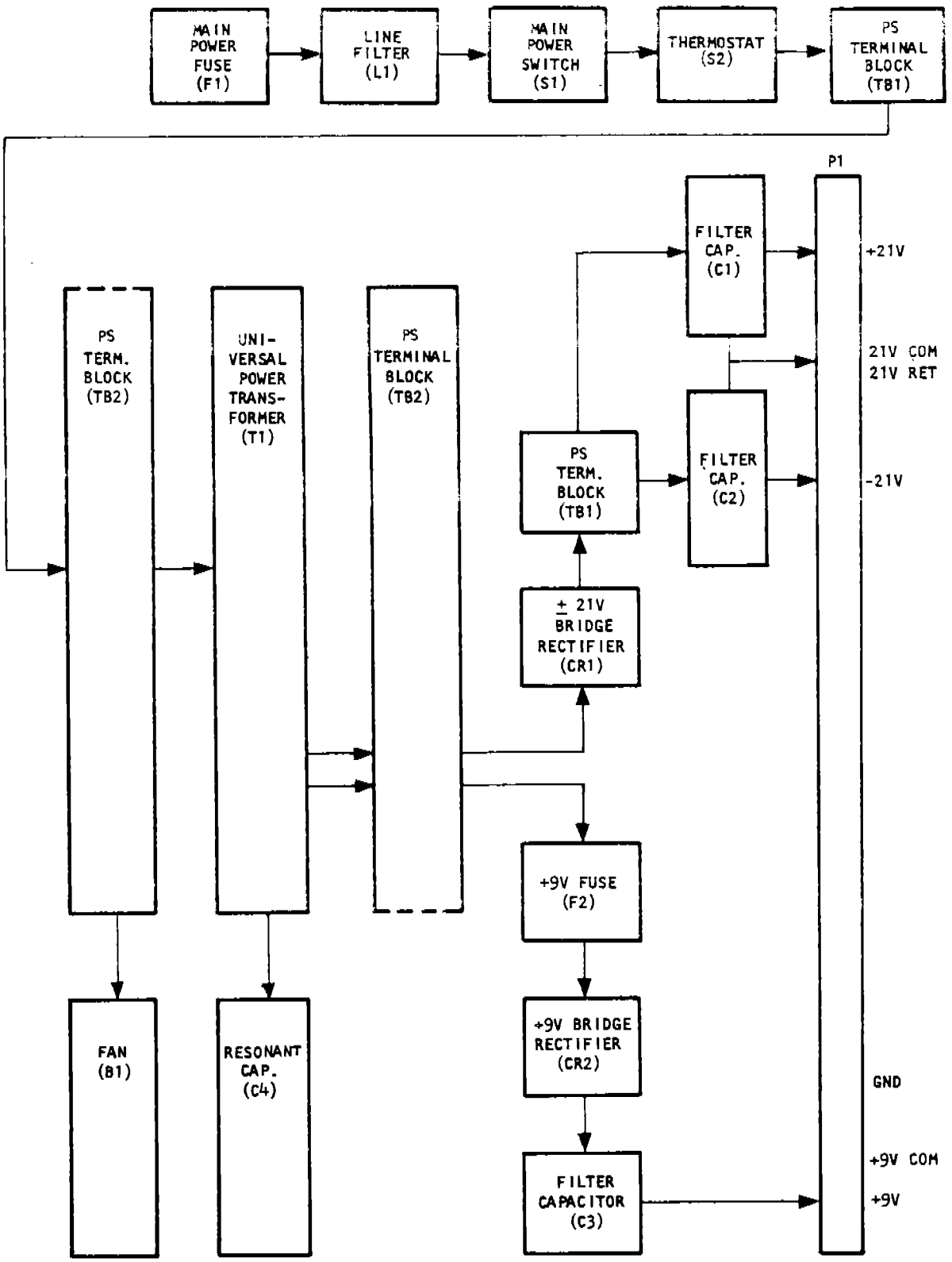



Figure 1-8. Universal Power Supply Block Diagram

| | | |
|---|---|---|
| Logic "1" | Signal: | Must be greater than +2.5 VDC and less than +5.5 VDC. |
| Logic "0" | Signal: | Must be equal to or greater than 0.0 VDC and less than +0.5 VDC. |

The Short Line Interface CCA receives standard codes in bit-parallel format. Data transfer between the user system and the printer is on a demand/response basis. Standard interface signals that the printer recognizes are listed below:

DATA STROBE
READY
ON LINE
DEMAND
DATA

Operation of the standard interface communications (handshaking) is as follows:

a. When the printer is able to be put on line by the operator, the READY signal goes active.

b. After the READY signal goes active, the DEMAND signal will go active to request data from the user.

c. In response to the DEMAND signal, the user will place data on the data lines and activate the DATA STROBE signal.

d. The printer samples and stores the character transmitted on the data lines.

e. Once the data lines have been sampled, the DEMAND signal goes inactive.

f. When the user detects that the DEMAND line has gone inactive, the STROBE signal can then go inactive.

g. Once the character has been stored, the printer verifies that the STROBE signal is inactive, then activates DEMAND again for the next character.

### 1.9.3 Processor Circuit Card Assembly (A3)

The Processor CCA is a microprocessor system which controls all functions of the printer, including character generation, paper motion, print head motion, data transfer functions, and operator controls. It allows for maximum print throughput by the use of bi-directional printing. The Processor CCA "looks ahead" at the next line of print to determine the proper starting point for minimum print head motion.

The Processor CCA includes a variable timing circuit which controls the period of time in which the wire driver circuits are turned on and off. Procedures for adjustment of this circuit are given in the M120/M200 Maintenance Guide, DPC 255074.

### 1.9.4 Motor Driver Circuit Card Assembly (A4)

The Motor Driver CCA provides the means of driving the three motors used in the printer: the shuttle servo motor, the paper feed stepping motor, and the ribbon drive motor.

The Motor Driver CCA controls starting, stopping, reversing, and velocity of the shuttle servo motor (B4) which drives the shuttle mechanism. A high efficiency power amplifier is used to drive the motor. Velocity information to the servo circuitry is provided by signals from the encoder disc mounted on the motor shaft. Motor stalling is detected and amplifier shut-down is automatically effected for safety purposes in the event that print head motion is impeded. This assembly also includes the adjustment for controlling the shuttle speed. Procedures for adjusting the speed control are given in the M120/M200 Maintenance Guide, DPC 255074.

The Motor Driver CCA also supplies the drive current pulses to the paper feed stepping motor (B2) to move the paper and to maintain the position of the paper during the print process.

Current for the ribbon drive motor is supplied from this assembly during printing operation. Ribbon motion occurs only when the shuttle servo motor and/or the paper feed motor is operating.

### 1.9.5 Wire Driver Circuit Card Assembly (A5)

This assembly supplies current to each of the print head solenoids as determined by control signals from the Processor CCA. The Wire Driver CCA also contains replaceable fuses for each pair of drive circuits. This prevents damage to the solenoids from excess current in the event of a malfunction.

### 1.9.6 Print Head and Shuttle Mechanism

The print head is mounted on a shuttle mechanism that is moved across the print line by a constant velocity DC servo motor. As the shuttle mechanism traverses the printing area, it is guided by means of two parallel bars. Two self-lubricating journal bearings hold the shuttle mechanism to the rear bar, while a single bearing guides the front edge of the shuttle mechanism along the second bar. This arrangement secures the print head in the proper relationship to the platen during printing operation.

The shuttle mechanism is moved bidirectionally at a constant velocity by the shuttle servo motor and belt. Constant tension is maintained on the belt by an idler pulley assembly. Column position information is obtained from an encoder disc mounted on the shuttle servo motor shaft. A transducer is used to indicate column one to ensure that the position information is properly referenced.

### 1.9.7 Ribbon Advance Components

The ribbon advance components consist of a ribbon cassette and ribbon drive motor. Both components are mounted on the shuttle mechanism and move together with the print head. The ribbon drive motor is energized only during printing and paper motion operations.

### 1.9.8 Paper Feed Components

The paper feed system consists of a paper feed stepping motor, paper feed drive belt, and tractor drive assembly. Driving power is supplied by the paper feed stepping motor, and coupled by the paper feed drive belt and tractor drive shaft to the tractors. The two tractors, located at either side and above the print station, move the paper vertically past the print head. A tensioning device, located below the print station, holds the form flat against the platen.

### 1.9.9 Control Panel

The control panel, located at the right front of the printer, contains all electronic controls and indicators necessary to operate the printer, with the exception of the main power switch/indicator. A ribbon cable connects the control panel to the printer control electronics, via the Mother Board CCA (A7).

## 1.10 SPECIFICATIONS

Table 1-1 summarizes the printer specifications.

TABLE 1-1. SPECIFICATIONS

| Item | Specifications M200 | Specifications M120 |
|---|---|---|
| Input Power Requirement | | |
| Universal: | 95 VAC to 140 VAC or 187 to 257 VAC | Same VAC; 50 or 60 Hz, ±1% single phase |
| Power Consumption | | |
| Idle: | 150 watts maximum | Same |
| Printing: | 275 watts maximum | Same |
| Temperature | | |
| Operating: | 10°C to 38°C (50° to 100°F) | Same |
| Storage: | -10°C to 50°C (14°F to 122°F) | Same |
| Transit: | -40°C to 71°C (-40°F to 160°F) | Same |
| Humidity | | |
| Operating: | 20% to 80%, non-condensing | Same |
| Storage: | 10% to 90%, 10% per hour | Same rate of change |
| Transit: | 98% maximum, 10% per hour | Same rate of change |
| Printer Dimensions | | |
| Height: | | |
| Cover closed: | 21.3 cm (8.38 inches) | Same |
| Cover open: | 57.1 cm (22.48 inches) | Same |
| Width: | 67.1 cm (26.4 inches) | Same |
| Depth: | 59.4 cm (23.38 inches) | Same |
| Power Cord Length | 4 meters (13.12 feet) | Same |
| Print Head Life | 300 million characters | 200 million characters |
| Ribbon Life | 5 million characters | Same |
| Printer Weight | | |
| Net: | 30 Kg (67 lbs) | Same |
| Shipping: | 37.2 Kg (82 lbs) | Same |
| Print Characteristics | | |
| Character Rate: | 340 characters per second nominal | 180 characters per second |
| Print Method: | Dot matrix, 7 horizontal by 7 vertical | Same |
| Printable Columns: | 132 columns maximum @ 10 cpi | Same |
| Pitch (Horizontal Spacing) | | |
| Standard: | 10 characters per 25.4 mm (1 inch); 132 characters/line maximum | Same |
| Condensed: | 16.7 characters per 25.4 mm (1 inch); 219 characters/line maximum | Same |
| Expanded: | 5 characters per 25.4 mm (1 inch); 66 characters/line maximum | Same |
| Interfaces | | |
| Standard: | Short-Line Parallel (maximum interface cable length of 15 meters) | Same |
| Options: | a. Long-Line Parallel (maximum interface cable length of 150 meters) | Same |
| | b. Serial (maximum interface cable length of 15 meters with RS232; 457 meters with current loop) | Same |
| | c. DPC Centronics-Compatible (maximum interface cable length of 15 meters) | Same |
| Line Spacing | | |
| Standard: | 6 lines per 25.4 mm (1 inch) | Same |
| Optional: | 8 lines per 25.4 mm (1 inch) | Same |
| Paper Feed | | |
| Slew: (Minimum slew rate) | 254 mm (10 inches)/second | Same |
| Step: (Single line advance) | 50 milliseconds maximum | Same |
| Throughput | | |
| Full Line: (132 characters) | 125 lines per minute | 75 lines per minute |
| Short Line: | 300 lines per minute | 200 lines per minute |
| Paper Form Requirements | Standard fan-folded, edge-punched | Same |
| Width: | 7.62 cm to 40.64 cm (3 inches to 16 inches) overall | Same |
| Length | The basic printer accommodates a 27.94 cm (11 inches) fixed form length | Same |
| | A 30.48 cm (12 inches) fixed form length is available as an option | Same |
| | Printers equipped with the optional forms length selector switch can accommodate 11 different form lengths ranging from 7.62 cm (3 inches) to 35.56 cm (14 inches) | Same |
| | Printers equipped with the optional TCVFU can accommodate forms lengths of up to 61 cm (24 inches) at 6 LPI, and up to 45.72 cm (18 inches) at 8 LPI | |
| | Printers equipped with the DAVFU option can accommodate forms lengths of up to 107 cm (42 inches) at 6 LPI, and up to 76.2 cm (30 inches) at 8 LPI | Same |
| Weight: | 36 G/M$^2$ (10 lb) minimum | Same |
| Thickness | 0.71 mm (0.028 inch) maximum | Same |
| Environmental Conditions: (Recommended operating and storage of forms for best printing) | 16°C (60°F), at a relative humidity of 40% to 60% | Same |
| Ribbon Selection Guide (Specifically qualified for matrix printing) | Fabric ribbon impregnated with non-fading ink, 12.7 mm (1/2 inch) by 36 meters (120 feet), continuous loop cassette | Same |

## 1.11 PRINTABLE FORMS

The printer is capable of printing on forms with as many as six parts. The duplicate parts may be printed on either carbonless paper or single shot carbon paper. Other multi-part forms may be used but should be tested under user operating conditions to verify proper paper handling and printout legibility. The recommended storage environment of the paper forms is 60°F (42°C) to 80°F (60°C) at about 40% to 60% relative humidity.

Table 1-2 lists the recommended form thickness and paper weights for both carbonless paper and single shot carbon paper. Lower paper weight forms may be used in all cases as long as the paper weight is above 10 pounds (37 grams per square meter) for any individual part.

The first column of table 1-2 is labeled "No. of Parts", and the numbers 1 through 6 represent the number of parts to a form. The "Form Part Location" heading is divided into six columns, each column corresponding to the page number of a multiple part form. Form Part Location column 1 represents the first part, or original copy, and is the copy closest to the print head after the form has been inserted into the printer and is ready for print.

The figures in each of the six Form Part Location columns are suggested paper weights for each form part, expressed in pounds and grams per square meter (gsm). Suggested total form thickness is given in inches and millimeters.

Example: For a carbonless three-part paper form, table 1-2 suggests the following weights:

Part 1 (in Form Part Location column 1) - 20 (75)
Part 2 (in Form Part Location column 2) - 15 (56)
Part 3 (in Form Part Location column 3) - 100 (163)*

* The 100 (163 gsm) is the weight for tab card stock, based upon paper dimensions of 24" x 36" per 500 sheets. All other weight values are based on paper dimensions of 17" x 22" per 500 sheets. A total thickness of all three example parts should be 0.014 inch (0.36 millimeter), as shown in the "Form Thickness" column of table 1-2.

NOTE

The heaviest weight form part should be the last page of a multiple part form located farthest from the print head when the form is inserted into the printer.

## TABLE 1-2. M-SERIES PRINTABLE FORMS

| Carbonless Paper | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| No. of Parts | Form Part Location | | | | | | Form Thickness | |
| | 1 | 2 | 3 | 4 | 5 | 6 | Inches | Millimeters |
| 1 | 100(163) | | | | | | .0070 | .18 |
| 2 | 20(75) | 100(163) | | | | | .0110 | .28 |
| 3 | 20(75) | 15(56) | 100(163) | | | | .0140 | .36 |
| 4 | 15(56) | 15(56) | 15(56) | 100(163) | | | .0175 | .44 |
| 5 | 15(56) | 15(56) | 15(56) | 15(56) | 20(75) | | .0170 | .43 |
| 6 | 15(56) | 12(45) | 12(45) | 12(45) | 12(45) | 20(75) | .0185 | .47 |

| Carbon Paper<br>Using 8 lb (19 gsm) Single Shot Carbon | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| No. of Parts | Form Part Location | | | | | | Form Thickness | |
| | 1 | 2 | 3 | 4 | 5 | 6 | Inches | Millimeters |
| 1 | 100(163) | | | | | | .0070 | .18 |
| 2 | 20(75) | 100(163) | | | | | .0130 | .33 |
| 3 | 20(75) | 15(56) | 100(163) | | | | .0180 | .46 |
| 4 | 15(56) | 15(56) | 15(56) | 100(163) | | | .0240 | .61 |
| 5 | 15(56) | 15(56) | 15(56) | 15(56) | 20(75) | | .0220 | .56 |
| 6 | 15(56) | 12(45) | 12(45) | 12(45) | 12(45) | 20(75) | .0240 | .61 |

## 1.12 OPTIONS

Options available with the M120/M200 printers are listed below and described in the following paragraphs:

a. Print Density Options
b. Format Control Options
c. Optional Interface Signals
d. Interface Connector
e. Long-Line Interface
f. DPC Centronics-Compatible Interface
g. Serial Interface
h. Automatic Line Feed
i. Elapsed Time Meter
j. Rear Forms Load
k. Pedestal
l. Ground Isolation
m. Seven-Bit Only Interface

### 1.12.1 Print Density Options

The printer can be configured to produce non-standard character and line spacing, as follows:

#### a. Condensed Character Spacing

This option allows the printer to print with a horizontal pitch of 16.7 characters per inch, in addition to the standard spacing of 10 characters per inch. A switch located on the Auxiliary Control Panel allows selection of either standard or condensed pitch. An octal 22 control code may be used to override this switch and enable condensed printing, regardless of switch setting. To reset the pitch to that established by the switch before override, any line terminator code may be used.

#### b. Selectable Line Pitch

This option allows the operator to select a vertical pitch of either 6 or 8 lines per inch by means of a switch located on the Auxiliary Control Panel. Selection of vertical pitch cannot be made by interface code. Underlining is not permitted when operating in the 8 lines per inch mode. Any underlined characters transmitted to the printer when 8 lines per inch is selected will be converted to blanks.

### 1.12.2 Format Control Options

The following format control options are described in this paragraph:

a. Fixed Form Length
b. Variable Perforation Skipover

c. Form Length Selector Switch
d. Tape Controlled Vertical Format Unit
e. Direct Access Vertical Format Unit

a. Fixed Form Length

The basic printer is configured to provide automatic Top of Form positioning when used with 11-inch forms. This feature may be optionally modified to allow use of 12-inch forms to suit international requirements. Requirements for operation with other form lengths can be met by the use of the Form Length Selector Switch or the Vertical Format Unit options.

b. Variable Perforation Skipover

The standard 3-line skipover distance may be modified to 0, 4, or 6-line skipover by means of the Option Configuration switches. The presence of either vertical format unit (TCVFU or DAVFU) transfers control of the skipover distance to the Bottom of Form and Top of Form data contained in the VFU memory.

c. Form Length Selector Switch

This option allows the operator to handle a variety of commonly used forms lengths and to automatically advance the paper to the top of form by means of an interface code or the TOP OF FORM switch on the Control Panel. Selection of one of eleven forms lengths is made by means of a rotary switch located on the Auxiliary Control Panel. The switch positions correspond to the forms lengths of 3, 3 1/2, 4, 5 1/2, 6, 7, 8, 8 1/2, 11, 12, and 14 inches. Letter designations A, B, C, D, and E are used for custom lengths. Unless configured for these custom lengths, use of these settings will result in a default of 11 inches.

d. Tape Controlled Vertical Format Unit (TCVFU)

The Tape Controlled Vertical Format Unit (TCVFU), consisting of an optical tape reader and associated electronics, is offered as an option to enable the handling of a variety of vertical formats, and to allow rapid paper slewing within individual formats.

Data is read from tape following each power-up operation, and stored in memory. The memory load will start when a hole is detected in the least significant tape channel (left-most), and continues until a hole is again detected in this channel.

Tape load operation is initiated by pressing the tape reader switch, located on the tape reader assembly, when the printer is in the off-line mode. VFU memory is loaded (1) when the printer is powered up, (2) following any tape change, or (3) following the detection of a VFU error. If an error occurs while loading tape, the ALARM indicator will light up. To recover from the error, the CLEAR switch must be pressed and the tape load operation repeated. At the end of the operation, the tape will come to a stop and the tractors will be synchronized with the memory at the Top of Form position.

Once the memory has been loaded, the tape reader turns off and all mechanical activity ceases. VFU instructions are transmitted to the printer by activating the Paper Instruction (PI) bit at the same time that coded instructions are presented on the data lines.

As paper is advanced, the buffer memory is electronically "rotated" in synchronization, as a tape loop would be rotated in a mechanical system. Turning off the power will result in loss of synchronization between form and TCVFU.

e. Direct Access Vertical Format Unit (DAVFU)

The Direct Access Vertical Format Unit (DAVFU) is offered as an option to enable handling of a variety of vertical formats, and allow paper slewing within a form in a manner identical to the TCVFU described above. Instead of loading the memory from a tape loop, the DAVFU provides for direct loading from the user system via the printer interface lines.

A DAVFU START code (156 octal) accompanied by print instruction signal PI, may be sent to the printer any time data is requested. Upon recognition of the DAVFU START code, subsequent codes are used to load the VFU memory rather than to cause printing or paper motion.

Once the number of memory positions corresponding to the length of form (252 lines maximum) has been loaded, a STOP LOAD code (157 octal) accompanied by paper instruction signal PI, is sent to the printer. This code causes the printer to return to the normal mode whereby all recognized codes are used for printing or paper motion. Once the memory has been loaded via the interface, DAVFU-controlled paper motion instructions and operation are identical to those of TCVFU.

Once the DAVFU is loaded, the Form Length Selector Switch and the Perforation Skipover feature are disabled. Perforation Skipover will occur whenever Bottom of Form (BOF) is detected and will stop when Top of Form (TOF) is detected.

1.12.3 Optional Interface Signals

The following optional interface signals are available with both the standard DPC Short-Line Parallel Interface and the optional DPC Long-Line Parallel Interface.

a. Parity Bit

This user-generated signal is used when Parity Error detection is required. If odd parity is selected, the PARITY BIT signal must be active when the total number of active high data bits (including the PAPER INSTRUCTION signal (if used) is even. If even parity is selected, the PARITY BIT signal must be active whenever the total number of active high data bits (including the PAPER INSTRUCTION signal, if used) is odd. Implementation of this option requires the OPTION HEADER.

b. Parity Error

This printer-generated signal informs the user that a parity error has been detected on interface data. The PARITY ERROR signal can be reset by either BUFFER CLEAR or a format code.

c. Paper Instruction

This user-generated signal informs the printer that information on the data lines is to be treated either as format data, or as a DAVFU start or stop code. This signal can only be used when the TCVFU or DAVFU option is installed; however, a line of data can be terminated, using the standard ASCII format codes (Paper. Instruction signal inactive) even though the TCVFU or DAVFU option is installed. The Paper Instruction signal is looked at only when the DEMAND signal is active.

d. Bottom of Form

This printer-generated signal is supplied to the user, and is active when the bottom of form (BOF) position has been reached. The BOF position is determined by the form length as wired in the standard printer, or as dictated by the TCVFU or DAVFU data when these options are enabled.

e. Top of Form

This printer-generated signal is supplied to the user, and is active when the top of form (TOF) position has been reached. The TOF position is determined by the form length as wired in the standard printer, or as dictated by the TCVFU or DAVFU data when these options are enabled.

f. Paper Moving

This printer-generated signal informs the user that the paper feed motor is energized.

### 1.12.4 Interface Connector

An optional 50-pin Winchester Connector is available. The Winchester mating connector and pins are not supplied with the printer.

### 1.12.5 Long Line Interface

The optional Long-Line Interface is a modified version of the standard DPC Short-Line Parallel Interface. It allows the user to communicate with the printer over an extended cable length of up to 492 feet (150 meters). Signals between the user and the printer should be transmitted over twisted pair wires, using 22 AWG wire with one to three twists per inch. In all other respects, this interface is identical to the standard DPC Short-Line Parallel Interface.

### 1.12.6 DPC Centronics-Compatible Interface

The DPC Centronics-Compatible Interface allows the user to interface with the DPC M200 printer in a manner compatible with Centronics printers. Data is transmitted over a short cable with a maximum length of 49 feet (15 meters), using twisted pair wires.

a. Logical Levels

Logical "1" = More positive than +2.4 VDC positive than +5 VDC.

Logical "0" = More positive than 0 VDC and less positive than +0.4 VDC.

Interface signals, with some exceptions, are active when in the logical "1" state. Exceptions: Signals DATA STROBE, ACKNOWLEDGE, INPUT PRIME, and FAULT are active when in the logical "0" state.

b. Interface Connector

The interface connector mounted on the printer is a 50-pin AMP HDP-20. Mating connector and contact pins are not supplied with the printer. An optional adapter cable that terminates in a Centronics-type 36-pin connector is available.

### 1.12.7 Serial Interface

The serial interface operates in an asynchronous receive-only mode, and may be used with or without a modem. Serial data is received from the user via current loop or standard EIA RS232 receivers. The interface will operate with a variety of baud rates ranging from 110 to 9600. Signals are transmitted over a cable with a maximum length of 50 feet (15.3 meters).

Logic Levels

RS232C

| MARKING<br>OFF | SPACING<br>ON |
|---|---|
| -3.0 VDC to -25 VDC | +3.0 VDC to +25 VDC |

20 mA Current Loop

| MARKING<br>IDLE | SPACING<br>BREAK |
|---|---|
| 17.0 mA to +20 mA | 0.0 mA to 1 mA |

a. Interface Connector

The interface connector mounted on the printer is a 50-pin AMP HDP-20. Mating connector and pins are not supplied with the printer. An optional adapter cable is available that terminates in a 25-pin AMP HDP-20 connector.

1.12.8 Automatic Line Feed

When implemented, this option allows a line feed to occur upon detection of a carriage return code at the interface. A line feed code will also cause a line advance. Implementation of this option requires the use of the Option Configuration Switches.

1.12.9 Elapsed Time Meters

This option provides two elapsed time meters which enable the user to measure both "power on" and "print time" within ±10% accuracy.

1.12.10 Rear Forms Loading

The printer may be optionally configured for rear forms loading. The standard front and bottom forms loading capability will not be affected.

1.12.11 Pedestal

A pedestal is available for those applications requiring a floor-mounted printer. It is shipped separately from the printer in a disassembled state to reduce shipping costs and storage space requirements. A shelf is attached to the rear of the pedestal providing for passive stacking of paper as it exits the printer.

1.12.12 Ground Isolation

The standard printer is shipped with logic and frame grounds interconnected. If ground isolation is desired, it may be accomplished by removing a jumper in the power supply.

1.12.13 Seven-Bit Only Interface

This option allows the printer to operate with a controller which is capable of providing only seven data bits rather than eight bits as required in the standard interface. When operating with this option, the character set is limited to 96 characters. Implementation of this option requires the Option Configuration Switches.

# SECTION II

# THEORY OF OPERATION

## 2.1 GENERAL

This section describes the functional and logical operations of the printer system. A description of the input data is provided, followed by two levels of circuit description: functional and detailed.

## 2.2 INPUT DATA DESCRIPTION

Data is transmitted from the user system in an 8-bit (7-bit optional) format. An optional ninth bit, termed PI (paper instruction) is used for coding certain types of paper motion commands and loading DAVFU format codes.

The DPC Parallel Interface is the standard interface. Three other types of interfaces are available on an optional basis: the Serial Interface, the DPC Centronics-Compatible Interface, and the Long Line Parallel Interface. Interface details are described in paragraph 2.4.

Regardless of the type of interface used, information carried by the data path includes print characters, ASCII-coded paper motion characters, VFU-coded paper motion characters, direct access VFU (DAVFU) data, and condensed and expanded print codes. A fifth type of information, SELECT and DESELECT codes, is reserved for use by the optional DPC Centronics-Compatible Interface. All print characters, some of the paper motion characters, SELECT and DESELECT codes, and condensed and expanded print codes are normally ASCII-coded. As an option, the user may transmit data in a code of his own choosing. A special code converter then translates the user-coded data into ASCII characters for internal use. Table 2-1 lists the ASCII-coded characters recognized by the printer.

## 2.3 FUNCTIONAL DESCRIPTION

Figure 2-1 is a functional block diagram of the major printer assemblies and components of the M-Series printers. Note the differences between the M200 and M120 printers. The assemblies shown include the Interface CCA, Processor CCA, Wire Driver CCA, Motor Driver CCA, operator control panel, shuttle servo motor and encoder, ribbon motor, and printer interlocks. In addition to the standard components, the printer may include two optional items: the tape controlled vertical format unit (TCVFU) and the option configuration switches. The following paragraphs describe the data flow and interaction among the printer components during different modes and phases of printer operation.

## Table 2-1. ASCII-CODED CHARACTERS

128 CHARACTER PRINTING SET

ASCII NON-PRINTING | ASCII 96 CHARACTER PRINTING SET

| b8 b7 b6 b5 / b4 b3 b2 b1 | 0 0 0 0 | 0 0 0 1 | 0 0 1 0 | 0 0 1 1 | 0 1 0 0 | 0 1 0 1 | 0 1 1 0 | 0 1 1 1 | 1 0 0 0 | 1 0 0 1 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 0 0 0 | | | SPACE | 0 | @ | P | \ | p | £ | Ã |
| 0 0 0 1 | | SELECT** | ! | 1 | A | Q | a | q | ¡ | Ñ |
| 0 0 1 0 | | CD* | " | 2 | B | R | b | r | ¤ | Õ |
| 0 0 1 1 | | DESELECT** | # | 3 | C | S | c | s | é | Ø |
| 0 1 0 0 | | | $ | 4 | D | T | d | t | u | õ |
| 0 1 0 1 | | | % | 5 | E | U | e | u | Å | ß |
| 0 1 1 0 | | | & | 6 | F | V | f | v | Y | ü |
| 0 1 1 1 | | | ' | 7 | G | W | g | w | ¬ | õ |
| 1 0 0 0 | | | ( | 8 | H | X | h | x | ò | æ |
| 1 0 0 1 | | | ) | 9 | I | Y | i | y | ¢ | ä |
| 1 0 1 0 | LF | | * | : | J | Z | j | z | u | á |
| 1 0 1 1 | | | + | ; | K | [ | k | ┤ | ñ | å |
| 1 1 0 0 | FF | | , | < | L | \ | l | ┘ | ↑ | S |
| 1 1 0 1 | CR | | - | = | M | ] | m | ├ | à | É |
| 1 1 1 0 | XP | | . | > | N | ^ | n | ~ | Ä | ç |
| 1 1 1 1 | | | / | ? | O | _ | o | SPACE | 'A' | Ç |

*CD IS DELETE CODE FOR DPC CONTRONICS-COMPATIBLE I/F ONLY
**SELECT AND DESELECT CODES FOR DPC CENTRONICS-COMPATIBLE I/F ONLY

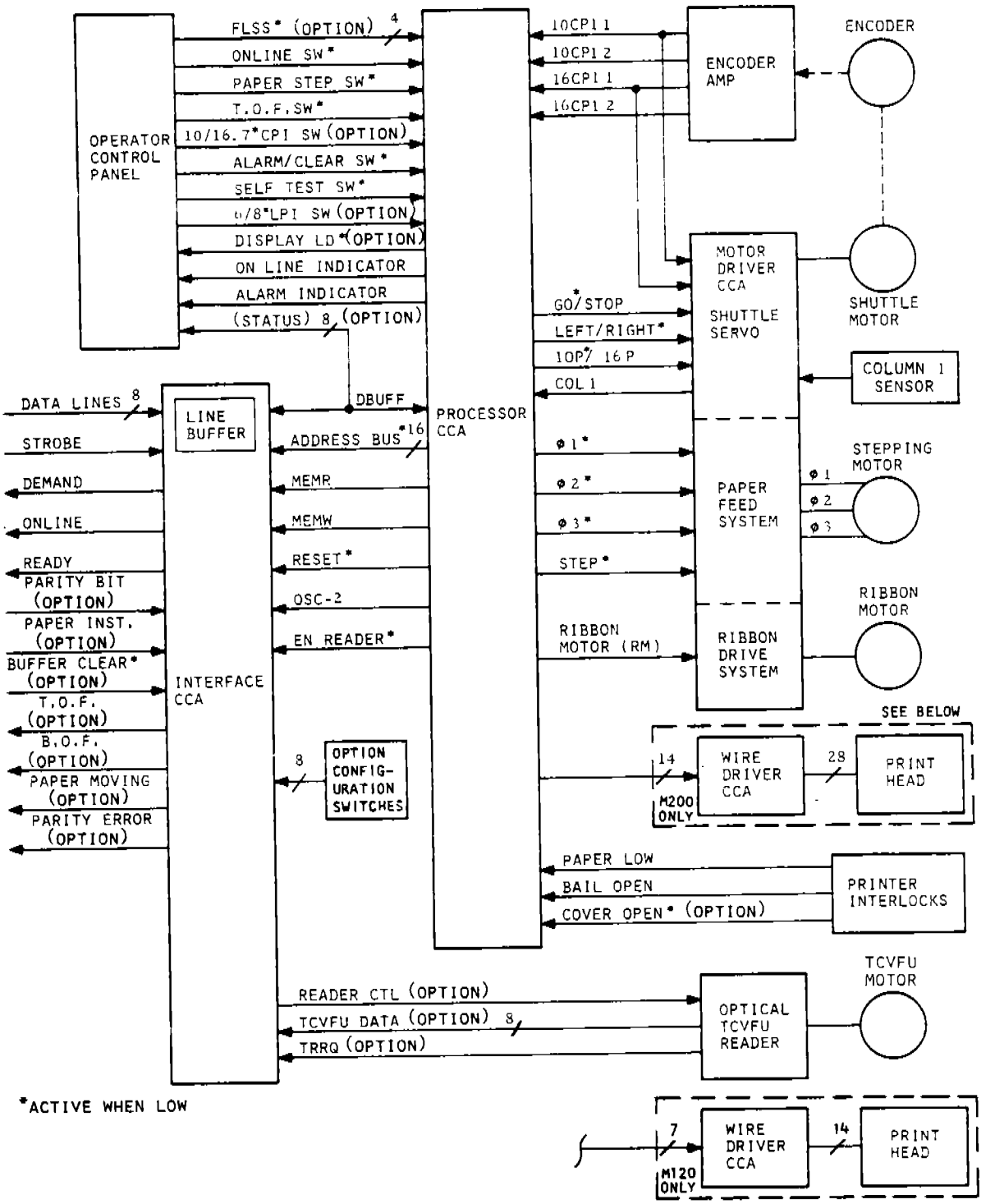



Figure 2-1. M-Series Printer, Functional Block Diagram

### 2.3.1 Modes of Operation

The printer operates in four basic modes, as follows:

Initialization

On Line

Self Test

Off Line

a. Initialization (Figure 2-2)

Figure 2-2 is a simplified flow diagram of activities that occur during the initialization mode of operation. Following power up, the printer enters the initialization mode of operation. During this mode, the Processor CCA locks the three-phase stepping motor in phase 1, stores the form length select switch (FLSS) information, reads the 10/16 CPI switch, and monitors the condition of the bail. If the bail is open, the ALARM indicator on the control panel will be turned on. The ALARM indicator will remain illuminated until the bail-open condition has been corrected.

The Processor CCA will then park the shuttle in the home position. To park the shuttle, the Processor CCA first checks the position of the shuttle with respect to column 1. If the shuttle is positioned to the left of column 1, the Processor CCA will signal the shuttle servo circuit within the Motor Driver CCA (via signals GO/STOP, LEFT/RIGHT) to move the shuttle to the right of column 1. If the shuttle is not positioned to the left of column 1 after the power is first turned on, the Processor CCA will signal the shuttle servo circuit to move the shuttle from right to left. Then, when column 1 is sensed, the Processor CCA will signal the shuttle servo circuit to reverse direction from left to right, and will again stop the shuttle servo motor to the right of column 1.

Direction of the shuttle servo motor travel and shuttle position is computed from information supplied by the encoder, which is mounted on the same shaft as the shuttle servo motor. When the shuttle servo motor travels, the encoder supplies a continuous stream of four output signals: 10CPI 1, 10CPI 2, 16CPI 1, and 16CPI 2. Only one pair of signals is used at any given time, depending upon the position of the optional 10CPI/16CPI pitch select switch. When the switch is not installed, the Processor CCA monitors signals 10CPI 1 and 10CPI 2. From these, the Processor CCA computes both direction of shuttle travel and shuttle position.

After the shuttle is parked, the Processor CCA monitors the position of the on line flip-flop. If the on line flip-flop is reset, off-line operations are performed. If the on line flip-flop is set, the position of the self test switch is monitored. Assuming that the self test switch is off, the printer interlocks are monitored for an out-of-paper condition. If the printer is out of paper, a paper empty status word is sent on the data bus to the control panel along with the DISPLAY LD signal. This will cause the optional status indicator to display a two-

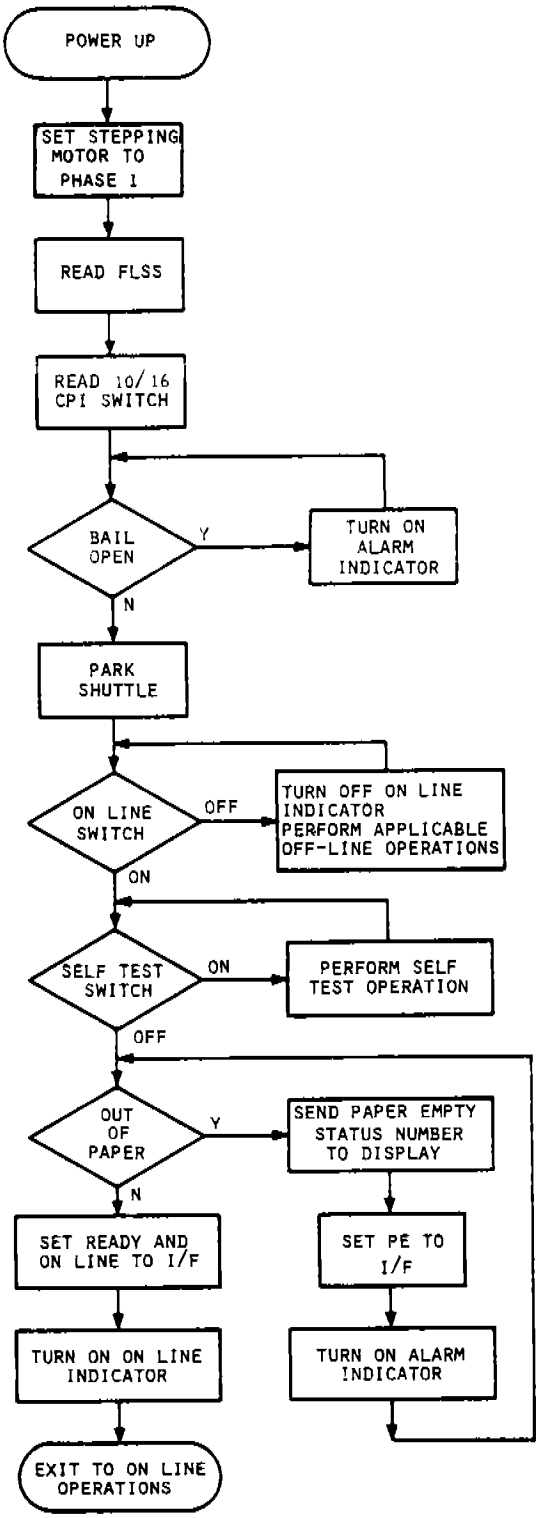



Figure 2-2. Initialization Mode of Operation

digit number that corresponds to the out-of paper condition. In addition, when an out-of-paper condition has been detected, a PE error signal is sent to the Interface CCA via the data bus, and the ALARM indicator on the control panel turns on.

After the out-of-paper condition has been eliminated, or if no out-of-paper condition existed in the first place, the READY and ON LINE signals are sent to the Interface CCA, and the ON LINE indicator is turned on. The Interface CCA then raises the READY and ON LINE signals to the user system.

b. On Line (Figure 2-3)

Figure 2-3 is a simplified flow diagram of the activities that occur during the on-line mode of operation, which include:

Load Buffer Cycle

Buffer Interrogate Cycle

Position Seek Cycle

Print Cycle

Paper Motion Cycle

The first event in the on line mode of operation, the load buffer cycle, is initiated when the Processor CCA transmits a load buffer signal to the Interface CCA and ends when the Interface CCA returns a buffer full signal. Along with the load buffer signal, the Processor CCA sets a load window timer. If the buffer full signal is returned before the timer expires, the Processor CCA will reset the load buffer signal, interrogate the line buffer, enter the position seek cycle, execute the paper motion command, and will then enter the print cycle. If the timer expires before the buffer full signal is received, the Processor CCA will stop the shuttle, execute the paper motion commands, and then wait for the buffer full signal. Upon receipt of the buffer full signal, the Processor CCA will reset the load buffer signal, interrogate the buffer, enter the position seek cycle, and enter the print cycle.

1. Load Buffer Cycle - Once initiated by the Processor CCA, the load buffer cycle is under control of the Interface CCA and is used to load user data into the line buffer. Typically, the user will transmit one line of 132 print characters, followed by a paper motion (control) character. Receipt of the paper motion character terminates the load buffer cycle, causing the Interface CCA to transmit the buffer full signal to the Processor CCA. In standard printers, each character is requested and strobed on a demand/strobe basis, transmitted over the eight data lines, and stored sequentially within the line buffer. In those printers configured with either the optiona' Serial Interface CCA or optional DPC Centronics-Compatible Interface CCA, communication and character transmission are as described in paragraph 2.4.

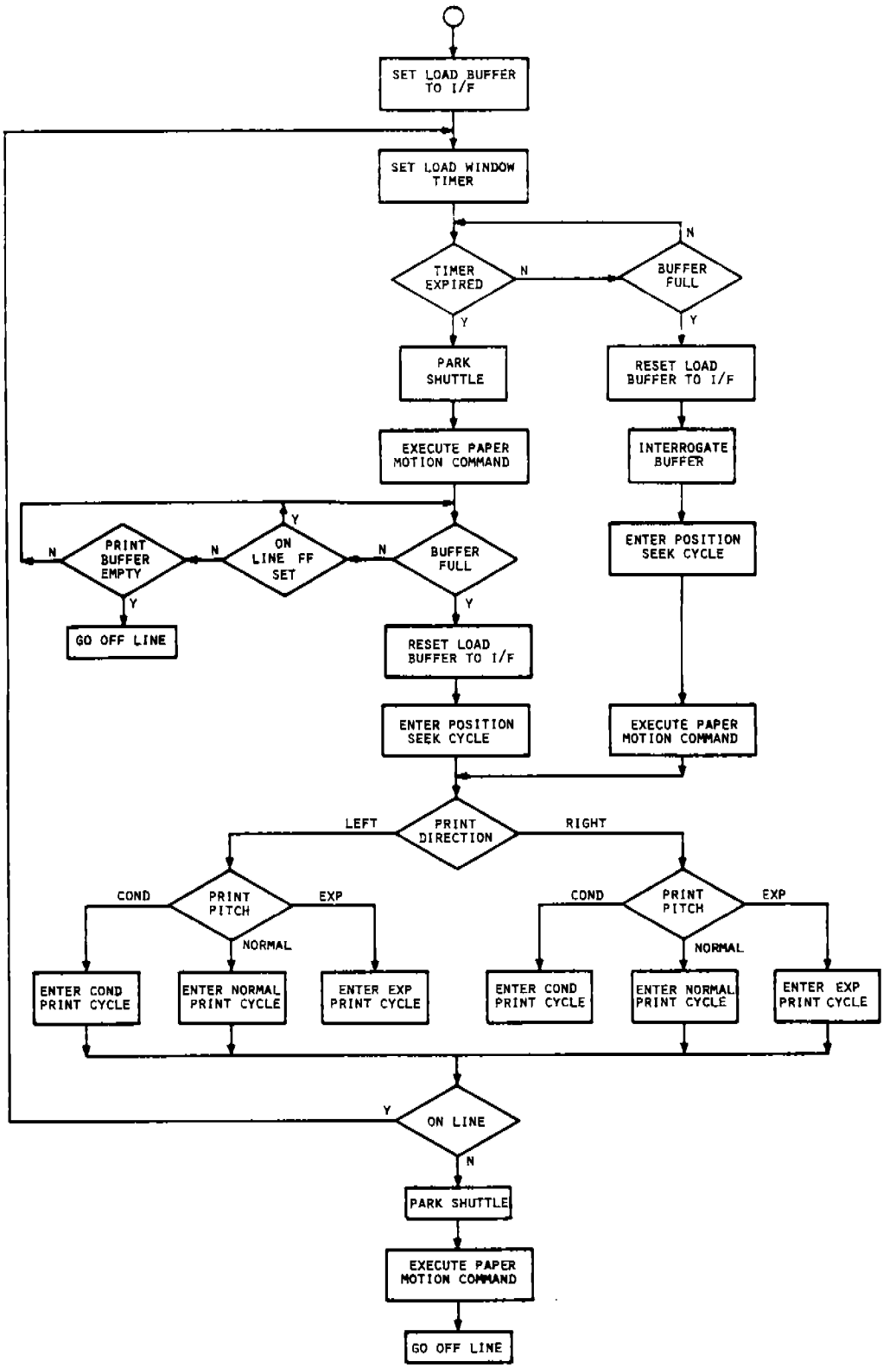



Figure 2-3. On Line Mode of Operation

2. Buffer Interrogate Cycle - During this cycle, the Processor CCA examines the contents of the line buffer one character at a time, starting with the last character loaded, and in a descending order. Each character found to be valid is restored to its original form. Non-printable characters are replaced by a question mark. Parity errors are replaced by a space code in the standard printer, and by a dollar sign in printers configured with a Serial Interface CCA. At the end of the buffer interrogate cycle, the paper motion character, the buffer address of the end of the line, and the buffer address of the beginning of the line are stored within the Processor CCA.

3. Position Seek Cycle - The position seek cycle is used by the Processor CCA to compute the print direction of the line of data received during the preceding load buffer cycle. To accomplish this, the Processor CCA first determines the current position of the shuttle. This information, along with the beginning and end of line information obtained during the buffer interrogate cycle, is then used to determine the most efficient direction for printing the upcoming line.

4. Print Cycle - The print cycle consists of three interrelated operations: shuttle motion, printing, and ribbon motion. Once started, shuttle motion is normally a continuous activity, lasting for the duration of the printing operation. Shuttle motion is under control of the Processor CCA. The Processor CCA uses the GO/STOP and LEFT/RIGHT signals along with 10P/16P to control the time, direction, and rate of shuttle travel to the shuttle servo circuit. In turn, the shuttle servo circuit supplies driving power accordingly to the shuttle motor. Exception: if more than one line of paper advance is executed, or if the buffer full signal from the Interface CCA is received after the load window timer has expired, shuttle motion will be interrupted and the shuttle will be stopped in its present position.

Printing involves converting the ASCII-coded print characters stored in the line buffer into dot patterns, and then selectively firing the print wires in the left and right wire columns of the print head. Assume that the computation made during the position seek cycle has resulted in a left to right print direction. Accordingly, the Processor CCA accesses, via the data bus, the first valid print character stored in the line buffer. Within the Processor CCA, the ASCII-coded character is converted into seven distinct dot patterns, one for each character column, and three blanks. The three blanks account for the intercharacter spacing. When the print head reaches the position where the first character is to be printed, the Processor CCA, via the Wire Driver CCA, selectively fires the print wires of the left and right wire columns. This procedure is repeated for each character until all valid print characters currently stored in the line buffer are printed.

Figure 2-4 is an example of a typical print sequence character in a line consisting of 14 print characters and a paper motion character. The first character in the line, the letter "F", is in buffer location 52, the last character, the letter "W" is in buffer location 65, and the control code is in buffer location 66. Direction of print is from left to right, determined during the position seek cycle. Accordingly, printing starts when the shuttle reaches character column 52, and the first character to be printed is the letter "F". Similarly, printing stops in column 65 with the letter "W". Note that when print direction is from right to left, printing starts with the letter "W" and ends with the letter "F".

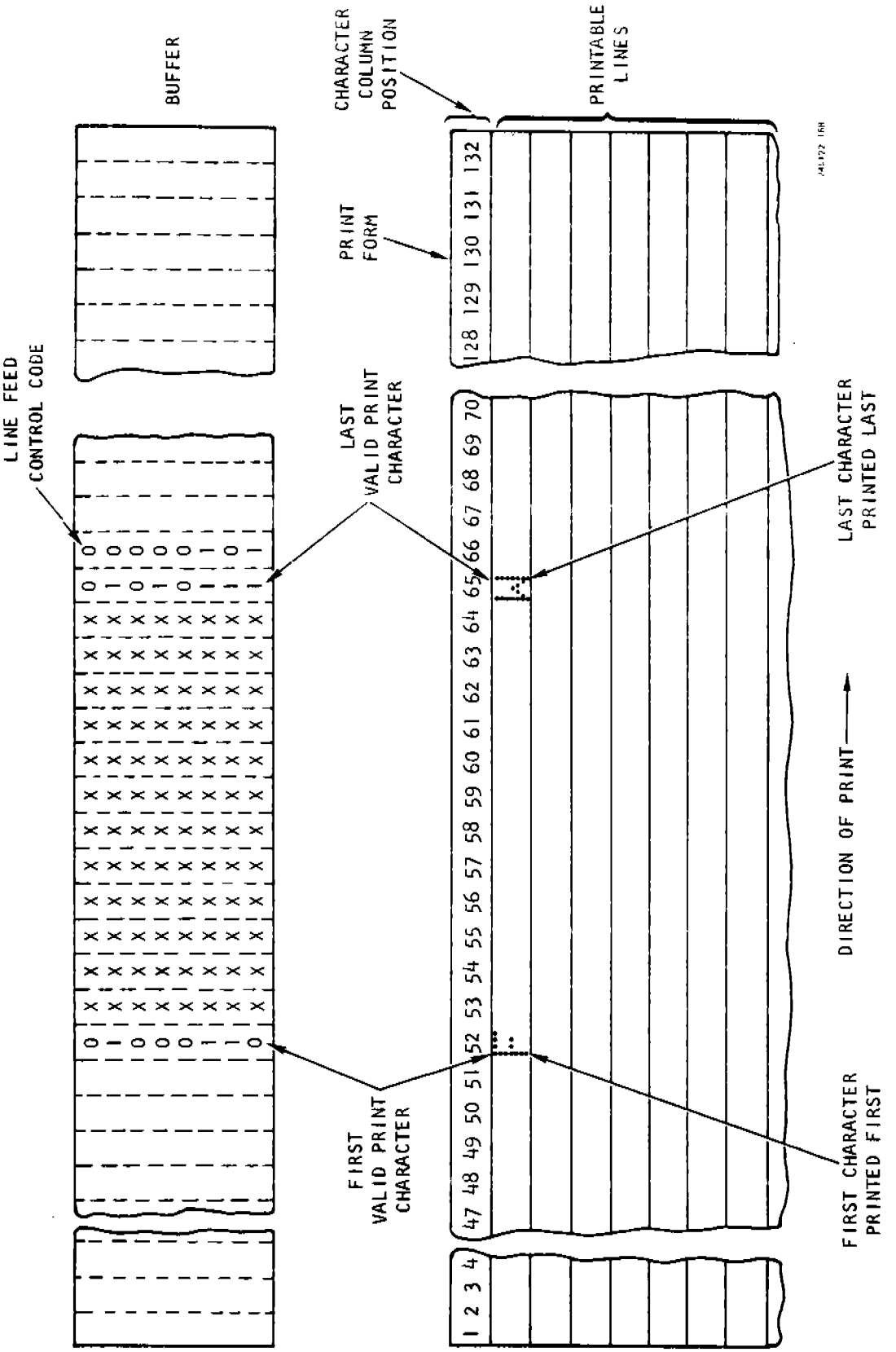



Figure 2-4. Typical Print Sequence

Character conversion and dot pattern generation in the M200 printer is implemented by a character generator ROM. As shown in figure 2-5, each of the 128 valid characters is assigned sixteen 8-bit ROM locations: eight locations for the right wire column, and eight locations for the left wire column. Only seven of the eight locations contain dot information; the eighth location is blank and forms one of the three intercharacter spaces. Information contained in a given location and identified in figure 2-5 by the letter "X" determines whether or not a dot is to be printed. Since there are only seven wires per wire column, bit 8 is always a blank. Each time a character is accessed from the line buffer, its ASCII code is used as a general address, pointing to eight locations within each half of the character generator ROM. One of eight locations is then selected by the column counter, a 4-bit BCD counter. When printing from left to right, the column counter is incremented from 0 to 9 with each encoder mark derived from the 10CPI 1/10CPI 2 (or 16CPI 1/16CPI 2) output of the encoder. Similarly, when printing from right to left, the column counter is decremented from 9 through 0 with each encoder mark. To account for the two additional intercharacter spaces (the other space is obtained from the blank column of the character generator), the character generator is not accessed. Instead, blanks are generated during counts 8 and 9 of the column counter when printing in either direction.

In the M120 printer, the print head has only one print column consisting of seven wires. Nevertheless, the character generator ROM is structured the same way as in the M200 printer; i.e. each valid character is assigned eight ROM locations for the right wire column, and eight ROM locations for the "left" wire column. Since there is no actual left wire column, information obtained from the left portion of the character generator is, under software control, automatically assigned to circuits controlling the right portion of the wire driver circuits.

Figure 2-6 is a simplified flow diagram of activities that occur during the print operation. For initial conditions, assume that the line buffer contains ten valid print characters in the first ten locations of the line buffer, that the column counter is at count 0, and that print direction is from left to right. When the first character is accessed from the line buffer, its ASCII code is combined with the dot column counter count to form a ROM address. This address is then used to access the character generator ROM to obtain the dot pattern of the first column of the first character. Next, the encoder mark is monitored. When the encoder mark occurs, the print wires are fired in a pattern corresponding to the pattern of dots contained in the addressed ROM location.

After the first column of the first character has been printed, and because the print direction is toward the right, the column counter is incremented to 1. Next, the column counter is tested for the counts of 0, 8, and 9. Since the count is 1, the sequence returns to access another location in the character generator ROM. Since the ASCII code did not change, the new location will contain the dot pattern for dot column 2 of character 1. After dot column 2 of character 1 has been printed, five more passes are made through the character generator ROM, printing dot columns 3 through 7. When the dot column counter reaches the count of 7, another pass is made through the character generator ROM. This time, no printing will occur, leaving column 8 of the first print character blank. On the counts of 8 and 9, the character generator is not accessed, and blanks are inserted in dot columns 9 and 10 of the first character.

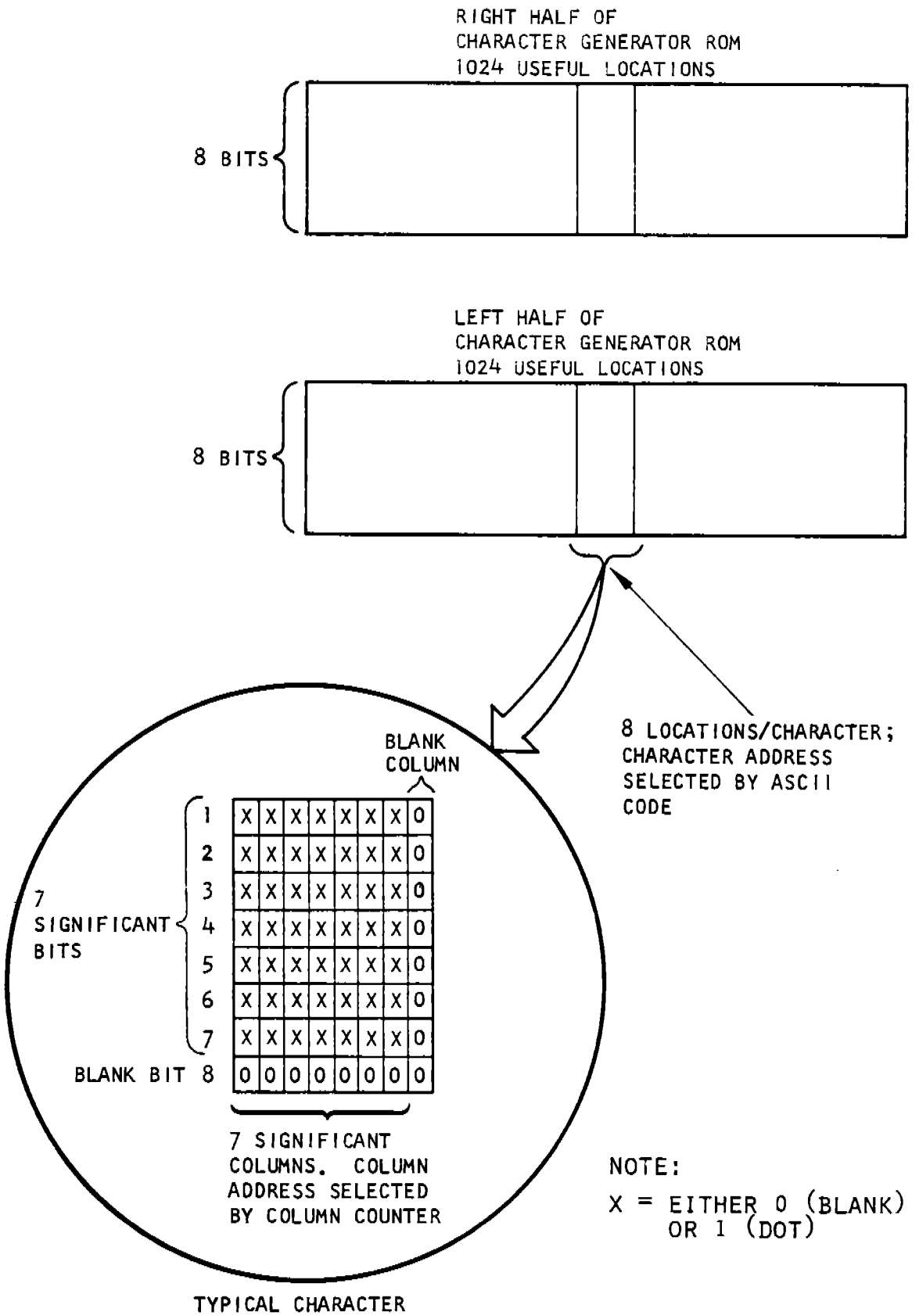



Figure 2-5. M200/M120 Character Generator ROM Structure

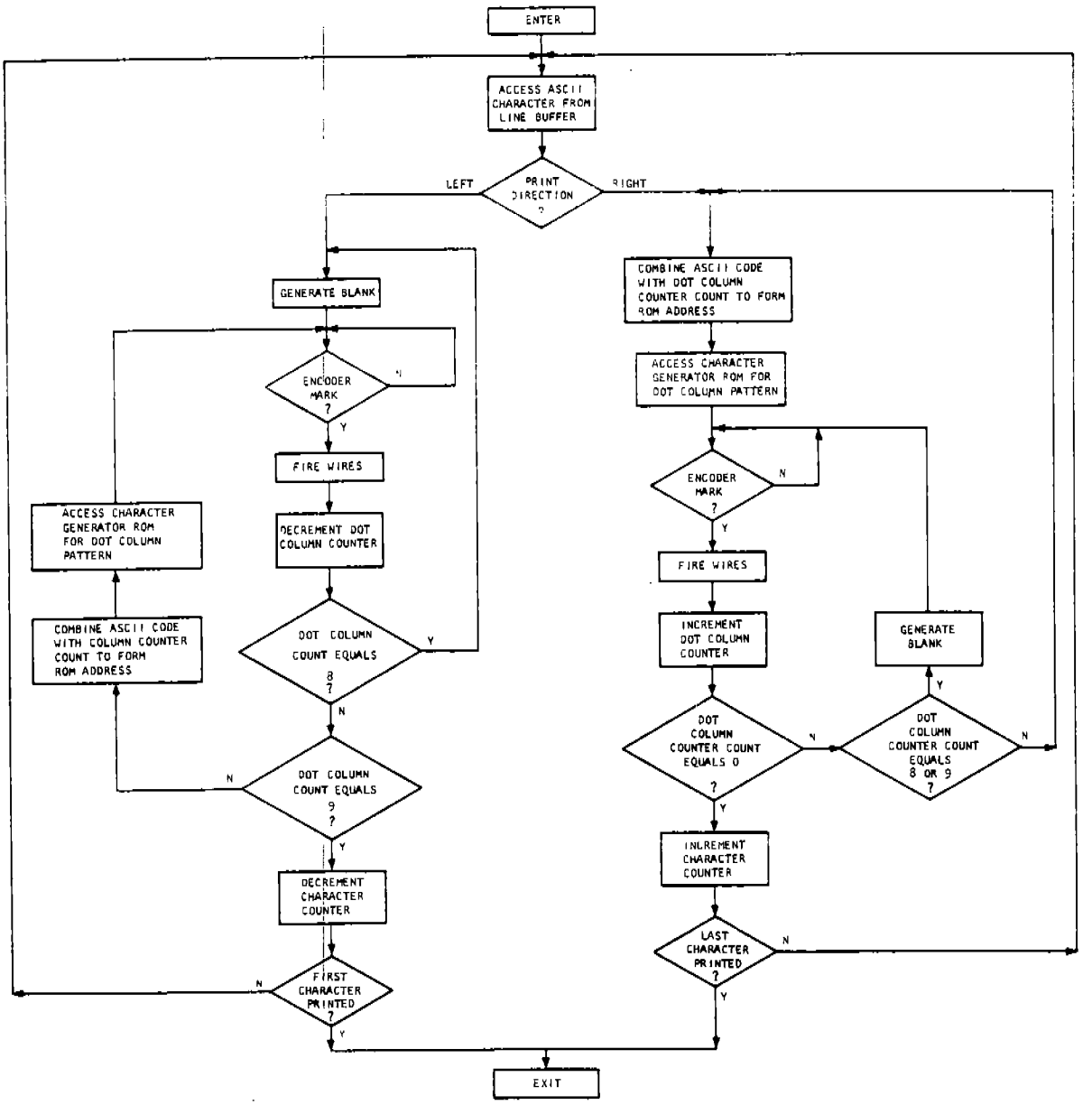



Figure 2-6. Print Operation, Simplified Flow Diagram

When the column counter is incremented from 9 to 0, the character counter is incremented, and a new ASCII-coded character is accessed from the line buffer. The entire sequence is repeated nine more times until all ten valid print characters are printed.

When printing from right to left, both the character counter and dot column counter start at the highest count, and are decremented during each applicable pass. Since the dot column counter is initially at 9, a blank is generated immediately, and also during the next pass when the dot column count is at the count of 8. On the count of 7, the character generator is accessed for the first time. When the dot column counter recycles from 0 to 9, the character counter is decremented and a new ASCII character is accessed. The print operation ends when the first and final character is printed. In all other respects, the sequence of events is the same as that of the left-to-right print operation.

Ribbon motion is initiated by the Processor CCA at the start of the print cycle through the ribbon drive system of the Motor Driver CCA, turning on the ribbon motor. Once started, ribbon motion is continuous for the duration of the print operation. Exception: as in the case of the shuttle motion, when the load buffer time exceeds the load window, ribbon motion is stopped and resumed at the start of the next print cycle.

5. Paper Motion Cycle - During the paper motion cycle, the command contained within the previously stored paper motion character is now executed. To do so, the Processor CCA decodes the paper motion character, and accordingly issues a series of stepping motor phase and step signals to the Motor Driver CCA. In turn, the Motor Driver CCA generates a series of stepping motor power signals. These signals are transmitted to the stepping motor, causing paper to advance a fixed number of lines (or one line).

c. Self Test

The self test feature provides the means of testing the printer under dynamic conditions. It operates with the printer on line and in the test mode (self test signal supplied by the control panel to the Processor CCA). However, the printer does not communicate with the user system. Instead, a fixed pattern of print and control characters is obtained from a memory area within the Processor CCA. In all other respects, the self-test operation is identical to a normal on-line operation. Once started, printing is automatic and continuous for 264 lines. After printing stops, the printer goes off line. To resume test operations, the operator must press the ON LINE switch on the control panel.

d. Off Line

When the printer is off line, the Processor CCA routinely checks the state of the various control panel switches. Two operations may be initiated at this time: paper step, and top of form. When the operator presses the PAPER STEP switch, signal PAPER STEP SW is applied to the Processor CCA. In turn, the Processor CCA, through signals 01, 02, 03, and STEP, turns on the stepping motor and causes paper to advance a single line. Similarly, when the operator presses the TOP OF FORM switch, signal T.O.F. SW causes the Processor CCA to turn on the stepping motor until the paper reaches the top of the next form. Pressing and

holding of either the TOP OF FORM or PAPER STEP switch will cause paper to advance continuously. To prevent the ribbon from smearing the paper, the ribbon drive system is active during the top of form operation.

### 2.3.2 Optional Printer Features and Components (Figure 2-1)

Optional printer components depicted in figure 2-1 and discussed in this paragraph include the Tape Controlled Vertical Format Unit (TCVFU) and the Option Configuration Switches. An optional feature, the Direct Access Vertical Format Unit (DAVFU), not shown in figure 2-1, is also discussed here. For a complete list of print options, refer to section I of this manual.

#### a. Vertical Formatting

Printers equipped with either a TCVFU or DAVFU option can accept a group of paper motion characters termed vertical format or VFU. These characters are not ASCII coded, but are accompanied by the optional print instruction signal PI. Upon recognition of the PI-coded paper motion character, the printer advances paper according to a pattern stored in the VFU area of the line buffer within the Interface CCA.

There are two categories of VFU-type paper motion characters, tape channel, and step count, as specified by bit 5 of the character. When bit 5 is a zero, paper is moved to a tape channel number specified by the value field encoded within the four least significant bits of the character. When bit 5 is a one, paper is advanced a number of lines encoded within the value field. Table 2-2 lists the binary codes used to transmit VFU-type paper motion characters.

#### b. TCVFU

The TCVFU option consists of an optical reader and motor. VFU information contained on the tape is loaded during the off line mode into the VFU area of the line buffer. Once loaded, the Processor CCA reads the VFU information directly from the line buffer, and the TCVFU becomes inactive. Note that the TCVFU option must be enabled by one of the option configuration switches.

To load VFU information from the tape to the line buffer, the operator first places the printer off line. Next, the operator presses a start switch on the optical reader, generating tape request signal TRRQ. Signal TRRQ is channelled through the Interface CCA and DBUF data bus to the Processor CCA. In response, the Processor CCA returns signal READER CTL through the data bus and Interface CCA, turning on the TCVFU motor. While the motor is running, TCVFU data is routed through the Interface CCA and over the data bus, one byte at a time, to the Processor CCA. From there, the TCVFU data is routed over the data bus and loaded in the line buffer. When all lines of the TCVFU tape are read and loaded, the Processor CCA disables the READER CTL signal, turning off the TCVFU motor.

**TABLE 2-2. VFU-TYPE PAPER MOTION CHARACTERS**

| Code | | | | | | | | | Command | |
|---|---|---|---|---|---|---|---|---|---|---|
| b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | PI | Description | Group |
| X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Move paper to Channel 1 | |
| X | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | Move paper to Channel 2 | |
| X | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | Move paper to Channel 3 | |
| X | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | Move paper to Channel 4 | |
| X | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | Move paper to Channel 5 | |
| X | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | Move paper to Channel 6 | Tape Channel |
| X | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | Move paper to Channel 7 | |
| X | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | Move paper to Channel 8 | |
| X | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | Move paper to Channel 9 | |
| X | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | Move paper to Channel 10 | |
| X | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | Move paper to Channel 11 | |
| X | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | Move paper to Channel 12 | |
| X | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | Move paper 0 line | |
| X | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | Move paper 1 line | |
| X | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | Move paper 2 lines | |
| X | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | Move paper 3 lines | |
| X | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | Move paper 4 lines | |
| X | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | Move paper 5 lines | |
| X | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | Move paper 6 lines | |
| X | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | Move paper 7 lines | Step Count |
| X | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | Move paper 8 lines | |
| X | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | Move paper 9 lines | |
| X | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | Move paper 10 lines | |
| X | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | Move paper 11 lines | |
| X | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | Move paper 12 lines | |
| X | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | Move paper 13 lines | |
| X | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | Move paper 14 lines | |
| X | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | Move paper 15 lines | |

X = Don't Care condition

c. DAVFU

Printers equipped with a DAVFU option are loaded with vertical format data by the user. DAVFU data, like print and paper motion characters, is transmitted over the 8-bit data path on a time-shared basis. The first character in a DAVFU stream is the DAVFU start code, which signifies that the next block of characters contains DAVFU tape channel information. The last character in a DAVFU stream is a DAVFU stop code, which marks the end of the DAVFU transmission cycle. DAVFU data is transmitted in pairs of characters. Therefore, the total DAVFU character count must always be even; an odd number of characters is interpreted by the printer as a DAVFU error.

d. Option Configuration Switches

The option configuration switches provide a means for configuring the printer with available options. Information from the option configuration switches is supplied on a 16 bit bus to the Interface CCA. Part of the information is used internally by the Interface CCA, while the remainder is routed over the data bus to the Processor CCA. Periodically, the Processor CCA examines the information supplied by the option configuration switches and accordingly, decides the manner in which data is to be processed.

## 2.4 INTERFACE DESCRIPTION

The standard M200 printer is designed to operate with a DPC Short Line 8-bit (seven bits optional) Parallel Interface CCA, and is configured with a DPC Parallel Interface CCA as depicted in figure 2-1. As an option, the printer can be configured to operate with a Serial Interface, with a DPC Centronics-Compatible Interface, or a DPC Long-Line Parallel Interface. To implement either option, the standard DPC Parallel Interface CCA is replaced with the applicable Interface CCA.

The Processor CCA cannot distinguish between a DPC Parallel Interface CCA and a Serial Interface CCA. Both CCAs connect to the Processor CCA through the same data and address buses and have identical bit assignments within the buses. Connections between the DPC Centronics-Compatible Interface CCA and the Processor CCA are also made through the same buses as the DPC Parallel and Serial interfaces. However, a selected number of bits have been assigned different functions to accommodate the special needs of the DPC Centronics-Compatible Interface.

Figure 2-7 shows the data and address buses that connect between the Processor CCA and any Interface CCA, and circuits that are common to any Parallel Interface CCA; the Serial Interface CCA uses a somewhat different scheme, and is described in detail in paragraph 2.4.2.

Also shown are the bit assignment differences between the DPC Centronics-Compatible Interface CCA and the other Interface CCAs. Information between the Interface CCA and Processor CCA is exchanged over a single 8-bit data bus DBUF1-DBUF8, buffered in the first bi-directional I/O port and then divided into three time-shared groups. One group is channeled by the second bi-directional I/O port, and includes all I/O data such as print, DAVFU, TCVFU, VFU, etc. The second and third signal groups are channelled, respectively, by the interface control latch and interface information latch, and together form a two-way communications path. The interface control latch stores input signals supplied by the Processor CCA, while the interface information latch stores output signals destined for the Processor CCA. Note the differences in bit assignments between the DPC Centronics-Compatible Interface CCA and the two DPC Interface CCAs. For example, bit 6 of the interface control latch is used for "paper moving" status with DPC-type interfaces, but it indicates a fault condition (LD) to a DPC Centronics-Compatible Interface. To differentiate between the two types of interfaces, the Processor CCA monitors bit 8 of the information latch; bit 8 is at ground level in the DPC Centronics-Compatible Interface CCA, and at +5V in the other two Interface CCAs.

In addition to the data bus, the Processor CCA supplies a 15-bit address bus (bit ADR10* is not used), along with signals MEMW and MEMR. Bits ADR11*-ADR15* are resolved in the chip select logic into chip select signals CS1-CS8, and are used within the Interface CCA to multiplex different devices that share a common data bus. Table 2-3 lists the function of each chip select signal.

**TABLE 2-3. CHIP SELECT FUNCTIONS**

| Signal | Binary Address | | | | | Function |
|---|---|---|---|---|---|---|
| | A15 | A14 | A13 | A12 | A11 | |
| CS1 | 1 | 0 | 0 | 0 | 0 | Allows the Processor CCA to write into or read from the line buffer. |
| CS2 | 1 | 0 | 0 | 0 | 1 | Allows the Processor CCA to read the last line-buffer address. |
| CS3 | 1 | 0 | 0 | 1 | 0 | Allows the Processor CCA to write into the interface control latch. |
| CS4 | 1 | 0 | 0 | 1 | 1 | Allows the Processor CCA to read the upper TCVFU bits. |
| CS5 | 1 | 0 | 1 | 0 | 0 | Not used. |
| CS6 | 1 | 0 | 1 | 0 | 1 | Allows the Processor CCA to read the interface information latch. |
| CS7 | 1 | 0 | 1 | 1 | 0 | Allows the Processor CCA to read the lower TCVFU bits. |
| CS8 | 1 | 0 | 1 | 1 | 1 | Allows the Processor CCA to read the option configuration switches. |

Signals MEMW and MEMR specify the direction of the data flow. Address bits ADR0* - ADR9* are used to specify the line buffer (not shown in figure 2-7) location when accessed by the Processor CCA.

The following paragraphs provide detailed information on each of the three Interface CCAs.

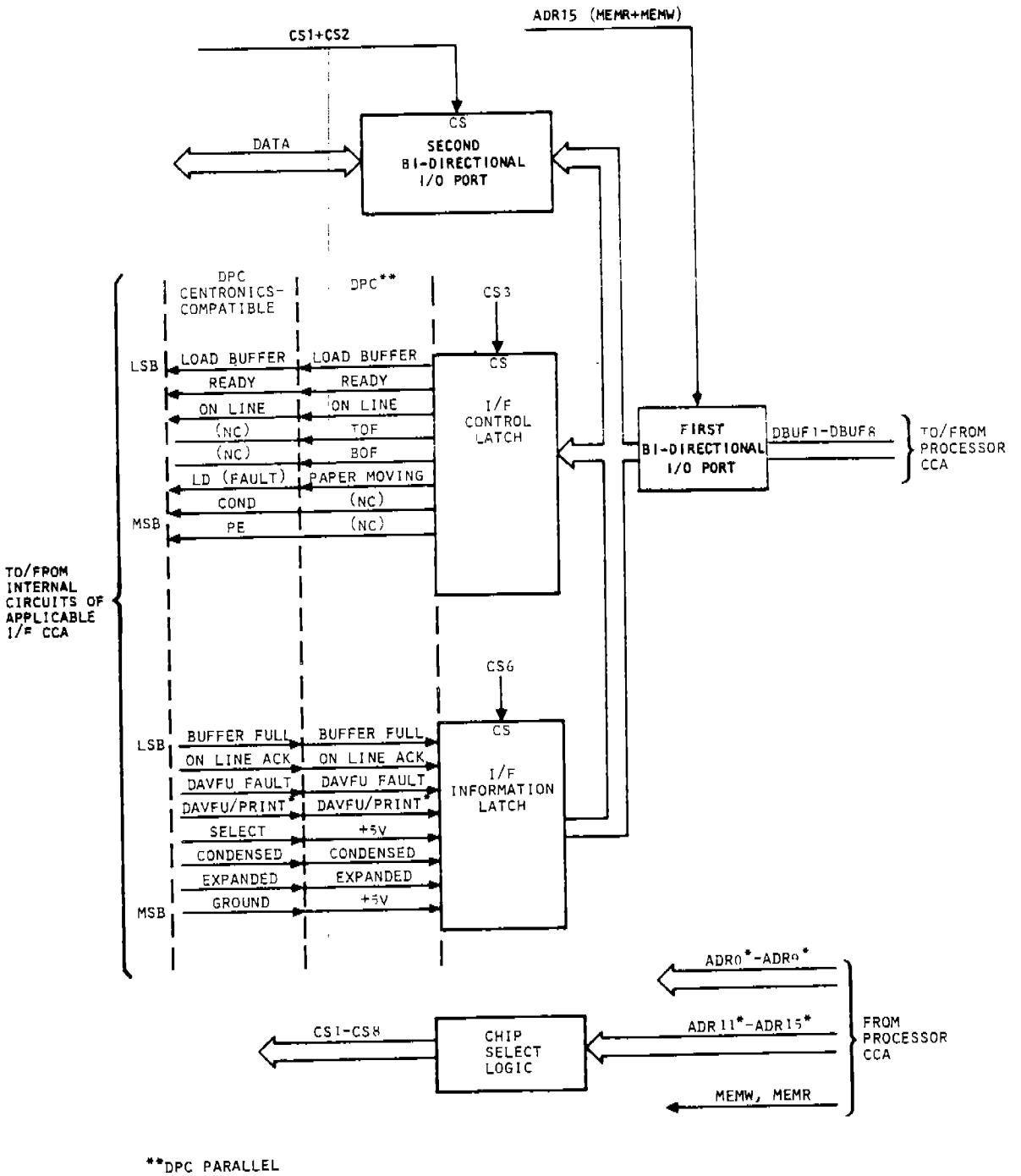



**Figure 2-7. Common Interface CCA Circuits**

### 2.4.1 DPC Parallel Interface (Figure 2-8)

NOTE

The following functional description applies to the standard, Short Line DPC Parallel Interface CCA, referred to as the Parallel Interface CCA in the following discussion. Except for additional input differential drivers and receivers, this description also applies to the optional, Long Line DPC Parallel Interface CCA.

The Parallel Interface CCA is designed to enable parallel data transfer between the user system and the Processor CCA. In addition, the Parallel Interface CCA provides the Processor CCA with information concerning print density, parity errors, system fault indications, on line/off line acknowledgement, and line buffer status.

a. Data Transfer Modes

Data transfer between the user system and the Parallel Interface CCA may be performed in two modes: normal, or fixed pulsed strobe mode. See figure 2-9 for the parallel interface timing relationships.

1. Normal Mode - In the normal mode of data transfer a demand/response or handshake technique is used which is initiated as follows: the Processor CCA generates clock signal OSC2. While the OSC2 clock is operating, the Processor CCA raises signal READY, fed out of control latch U33 under the control of signals CS3* and MEMW*. When signal READY is high, the Processor CCA raises signal ON LINE, also fed out of control latch U22.

Next, the Processor CCA initiates the data transfer by raising LOAD BUFFER, also fed out of control latch U33. At this time, the Parallel Interface CCA interface communications circuit generates signal DEMAND during the trailing edge of clock OSC2. While signal DEMAND is high, signal USER DEMAND is raised. The user system is requested to transmit signal DATA STROBE, which is raised at the same time that print data characters or paper motion characters (represented by data bits DATA01 - DATA08) are received on the leading edge of clock OSC2. Signal DATA STROBE clocks an internal strobe signal STBINT*, which goes low at the same time that signal DATA STROBE goes high. Signal STBINT* affects the operation of the WRITE* signal and the loading of the line buffer, discussed in subsequent paragraphs.

2. Fixed Pulse Strobe Mode - The fixed pulse strobe mode of data transfer is similar to the normal mode, with one exception: when the printer raises DEMAND to request data, the user may respond by pulsing and dropping the DATA STROBE signal. This way, DATA STROBE drops while DEMAND is still high; i.e., before the character is stored in the line buffer. In such cases, the Interface CCA acknowledges DATA STROBE immediately to the user, but also generates a strobe signal for internal use termed STBINT*. This strobe signal is delayed until DEMAND drops; i.e. until the data character is stored in the line buffer.

b. Chip Select Signal Generation

Chip select signals CS1* through CS4* and CS6* through CS8* are generated by chip select generator U22 from the five most significant bits of the Processor CCA's address input, ADR11-ADR15. These signals, in combination with MEMW and MEMR, are used to selectively enable different devices throughout the Interface CCA. Refer to table 2-3 for the function of each chip select signal.

c. User Input Character Transfer

Print, paper motion, or tape channel characters are obtained from the user on data bits DATA01-DATA08, routed through data inverter U36/U29 and data driver U42, and strobed into data latch U43 by signal data STB. From data latch U43 the character is transferred to one of two destinations: ASCII driver U45 and code converter MEM1.

Assume first that code conversion was not selected (signal code CONV* inactive). Accordingly, ASCII driver U45 is enabled and MEM1 is disabled, and the character is routed in its original form to data bus DB1-DB8. The expression LOAD.PARITY FLT* specifies that the data transfer occurs during the load cycle only, and that no parity error exists. Characters with a parity error are replaced by a blank, implemented in a circuit not shown in figure 2-8.

If code conversion is selected (CODE CONV* active), the characters are transferred to an optional code converter PROM, MEM1, which encodes the characters into an equivalent ASCII format. While MEM1 is enabled ASCII driver U45 is disabled. The output of either ASCII driver U45 or code converter MEM1 is fed into the line buffer locations specified by address bits 1 through 10 obtained from address counter driver U55.

d. Line Buffer Operation

Line buffer U39/U47 is a 1K by 8 RAM used to store ASCII-coded print data and vertical format data characters. Data may be written into the line buffer by either the Processor CCA or Parallel Interface CCA. Data is read out of the line buffer only by the Processor CCA. The Parallel Interface CCA may write into the line buffer by using signal WRITE for enabling purposes. The Processor CCA may write into the line buffer by using signals CS1, LOAD* and MEMW, and may read from the line buffer by using signals CS1, LOAD*, and MEMR. The term LOAD* prevents the processor from accessing the line buffer while it is being loaded with user data. Data between the processor and line buffer is routed through bus DBUF1-DBUF8, first interface port U57, and second interface port U49. Port U57 is enabled by the expression ADR15 (MEMR + MEMW), where MEMR and MEMW control direction of data flow. When MEMR is active, data flow is from the line buffer to the processor, and vice versa. Port U49 is controlled by the expression (CS1* + CS2*) MEMW*. Here too, the state of MEMW* controls direction of data flow. When MEMW* is active, data flow is from the processor to the line buffer.

When loading user data, nine of the ten line buffer address bits are supplied by the character counter on lines ACBIT1 - ACBIT9 through address count driver U54. The tenth address is obtained from U31/U23. When the line buffer is either read or written into by the Processor CCA, addressing is controlled by Processor address bits ADR0* - ADR9*, through Processor address port U56.

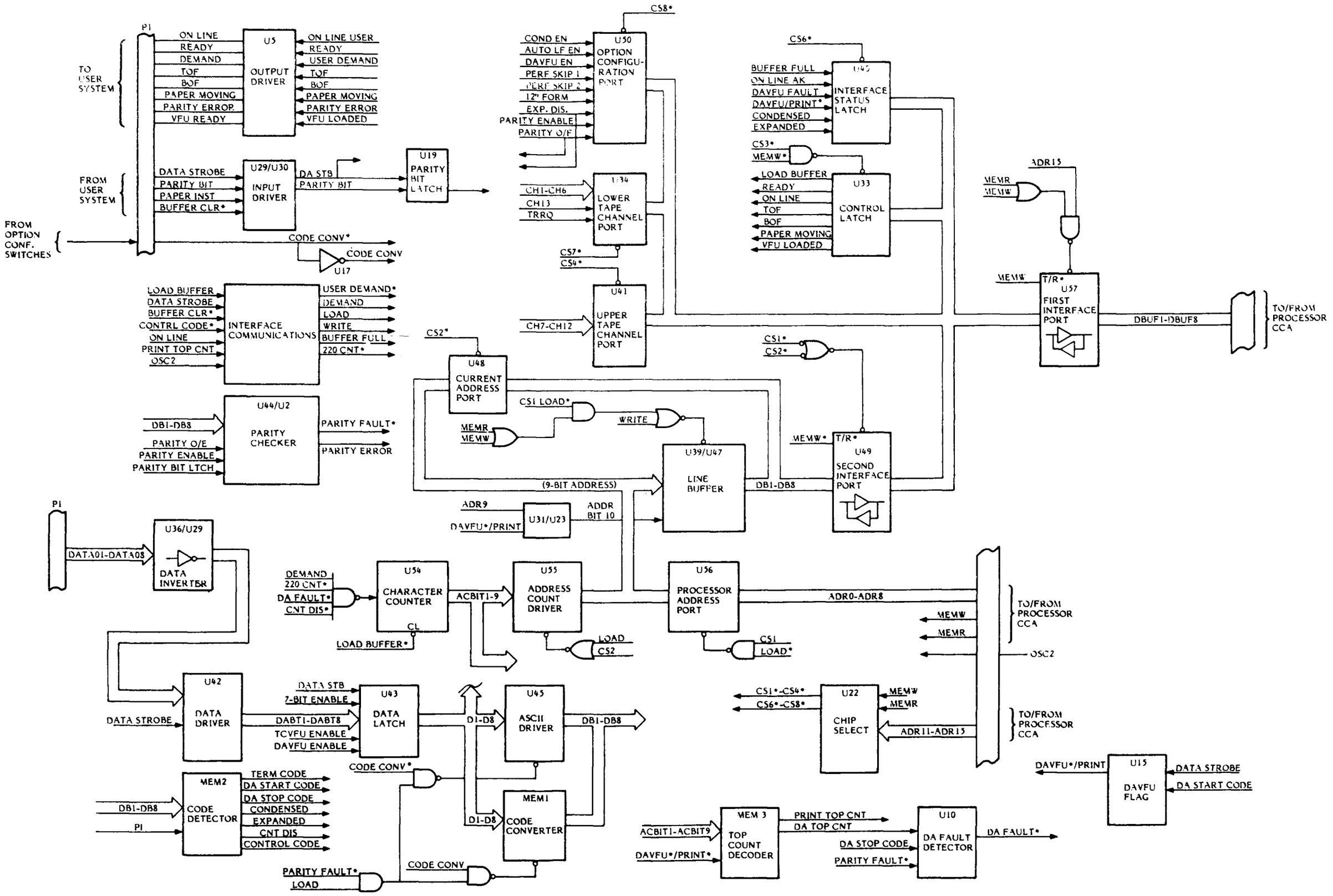



**Figure 2-8. Short Line Parallel Interface CCA Block Diagram**

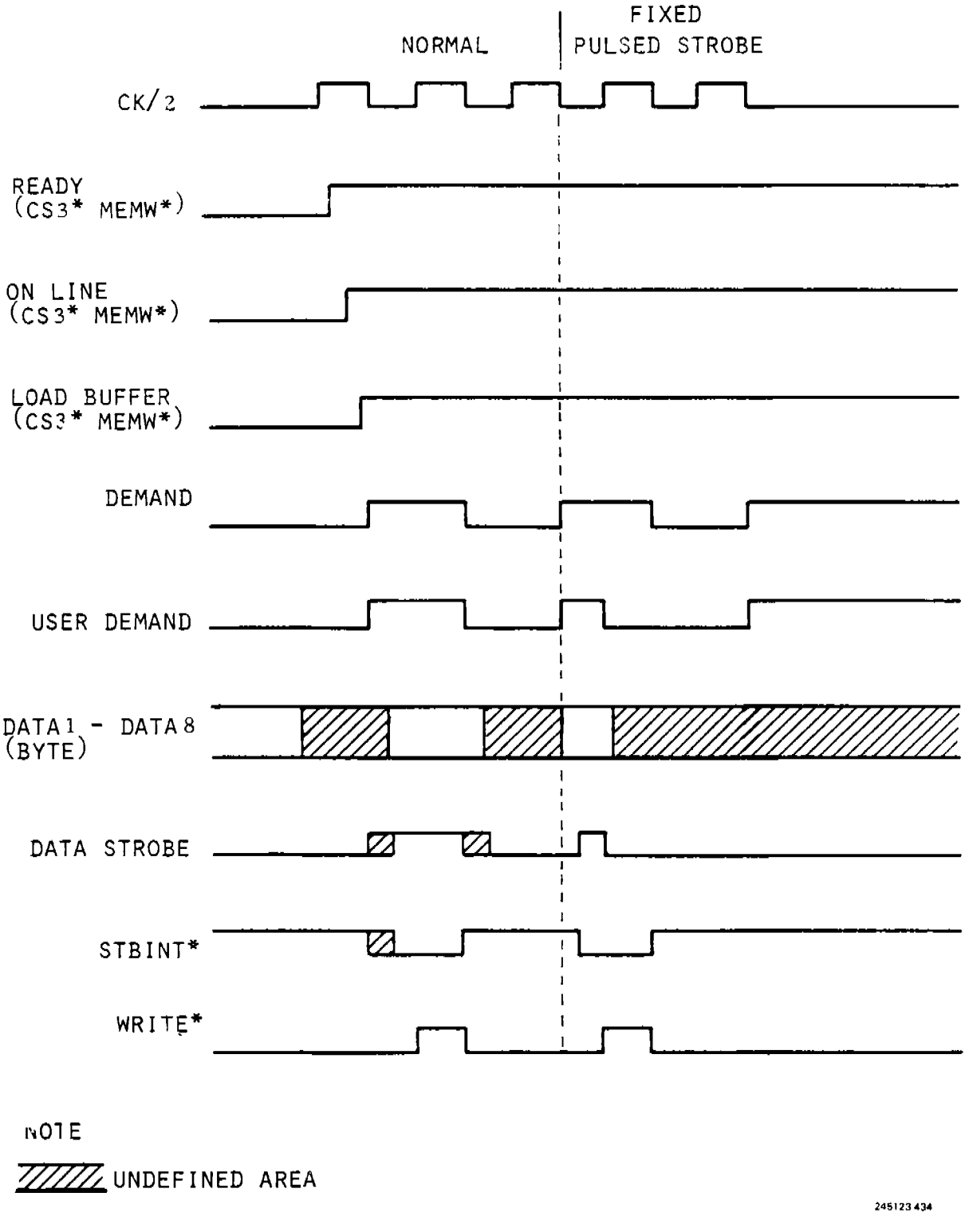



Figure 2-9. Parallel Interface Timing Diagram

1. Line Buffer Loading Completed - After loading a line of print data into line buffer U39/U47, the user system must send a paper motion control code to terminate that line. Control code decoder MEM2 issues signal CONTROL CODE*, causing the interface communication circuit to generate signal BUFFER FULL*. Signal BUFFER FULL is routed through processor interface status latch U40 to bus DBUF1-DBUF8, thereby informing the Processor CCA that the load operation has been completed.

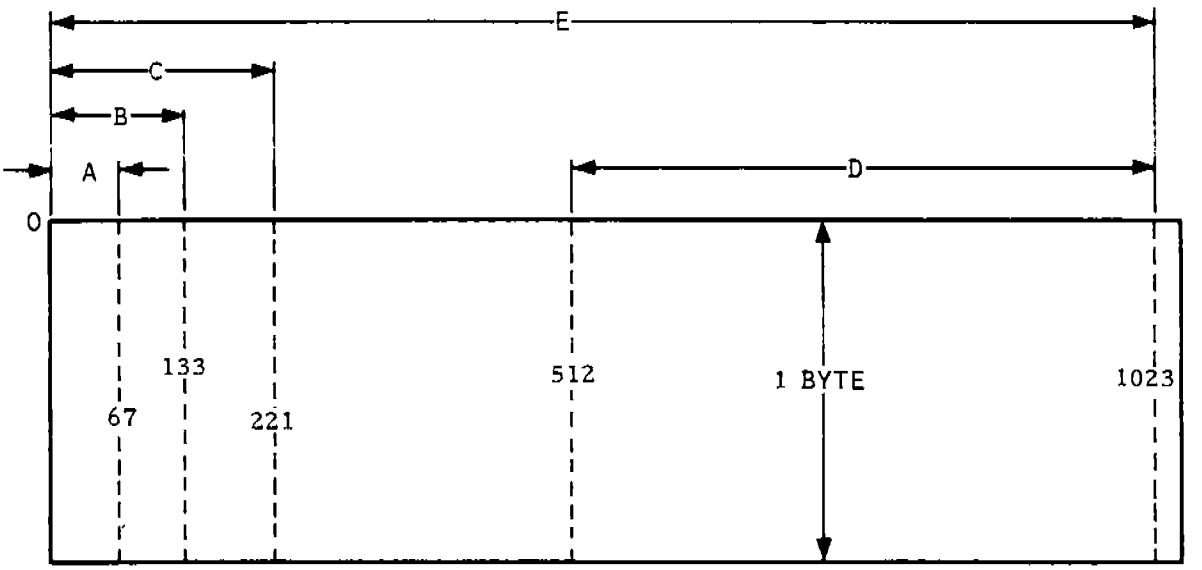
2. Line Buffer Interrogation - In order to read from the line buffer memory locations, the Processor CCA must determine the beginning and end of the line just stored. To do so, the Processor CCA first reads the current address counter count, using the expression CS2* to enable both address count driver U55 and current address pointer U48. Since the last character location on a line of print is the paper motion control code, the Processor CCA knows where the end of the line is.

3. Line Buffer Address Counting - Character Counter U54 provides the location address for the line buffer when loading user data. A line may have up to 132 print characters and one control code. Character counter U54 is a 9-bit binary counter which is cleared by signal LOAD BUFFER* when low. Provided that signals 220CNT*, DAVFU FAULT* and CNT DIS* are high, signal DEMAND will initially preset the address counter to a count of one before the user input character is received (signal DATA STROBE not raised yet). Each time that signal DEMAND is raised, the address counter will be incremented by one count.

Figure 2-10 is a memory map of line buffer U39/U47. Location 0 is used for Processor CCA testing. Locations 1 through 222 are dedicated for print data and format control characters. Locations 223 through 511 are not used. Locations 512 through 1022 are dedicated for TCVFU or DAVFU characters. Note that the actual print data and format control character location is dependent upon the print density in use. If normal printing is used, 132 print data characters plus one paper motion control code character will make the maximum characters (total characters per line to be printed) total 133. If optional expanded printing is used, the maximum number of characters will be 67. For optional condensed printing, the maximum number of characters will be 221.

The maximum number of print data characters per line may not always be used. A terminating code is sent by the user system whenever a line of print data is completed, and that code will add one additional character to the total character count. For example, if in the normal printing mode 70 print characters were sent by the user system, a total count of characters would be 71. Total memory space allotted for TCVFU or DAVFU characters is 512, spread over locations 512 through 1023. Not all locations are used.

4. Maximum Count - The DPC Short-Line Parallel Interface CCA can accept a maximum of 220 print characters per line, and a maximum of 510 DAVFU characters per DAVFU load operation. Characters beyond the number of 220, or 510 when loading DAVFU data, are not registered. This function is implemented by top count decoder MEM3, a 256x4 PROM. MEM3 monitors the address counter bits ACBIT1-ACBIT9 along with signal DAVFU*/PRINT. When signal DAVFU*/PRINT is high, MEM3 generates signal PRINT TOP COUNT when the count reaches 220. Similarly, when signal DAVFU*/PRINT is low,




NOTE

1. A = LOADING PRINT DATA (EXPANDED)
2. B = LOADING PRINT DATA (NORMAL)
3. C = LOADING PRINT DATA (CONDENSED)
4. D = LOADING TCVFU OR DAVFU DATA
5. E = TOTAL MEMORY SPACE
6. LOCATION ZERO IS USED FOR TESTING ONLY

Figure 2-10. Line Buffer Memory Location Mapping

MEM3 generates signal DA TOP COUNT when the count reaches 510. These top count signals prevent the excess characters from being written into the line buffer by inhibiting WRITE. In addition, these top count signals, through signal 20CNT*, disable the input to character counter U54.

5. DAVFU Fault Signal Generation - DAVFU fault signal is generated by fault detector U10 under one of three conditions:

Excessive number of characters
Odd Number of characters
Parity error (if parity option is installed).

6. DAVFU Character Storage - DAVFU characters are stored in the upper half of the line buffer storage area, locations 512 through 1022. To this end, circuit group U31/U23 monitors signal DAVFU*/PRINT. When signal DAVFU*/PRINT is low, indicating that the printer is receiving VFU tape channel characters, U31//U23 drives the most significant line buffer address bit high. With the most significant address bit high, the lower half of the line buffer locations is disabled.

e. Parity Checking

When optional parity checking is enabled, the user system adds a parity bit to the complement of data bits and PI bit, if any. Parity checker U44/U2 monitors the odd/even content of the character bits along with the parity bit. If the content is different from that specified by odd/even parity selection signal PARITY O*/E, two signals are generated: PARITY FAULT, and PARITY ERROR. Signal PARITY FAULT is used in ASCII driver U45 to replace the character that caused the fault with a blank. Signal PARITY ERROR is transmitted as a status signal to the user. In addition, it is used to set fault detector flip-flop U10. Note that signal PARITY FAULT is either set or reset once per character, whereas signal PARITY ERROR is reset once per line.

f. TCVFU Operation

The TCVFU option allows vertical format data from a punched paper tape to be routed to the Processor CCA. Data is routed from TCVFU ports U34/U41 through first interface port U57 and over the DBUF1 - DBUF8 bus. Since there are 12 TCVFU data channels plus a TRRQ (Tape reader request) channel, the Processor CCA must read each TCVFU character in two steps. Lower TCVFU channel signals CH1 - CH6, plus CH13, (representing a sprocket clock), and TRRQ (Tape reader request) are routed through lower tape channel port U34. Upper TCVFU signals CH7 - CH12 are routed through upper tape channel port U41. The Processor CCA utilizes chip select signals CS7* and CS4* to access TCVFU data. However, to transfer the TCVFU data from the tape reader to the Processor CCA, the printer operator must press the READ pushbutton located on the tape reader. This action sends the TRRQ signal to the Processor CCA via the DBUF1 - DBUF8 bus U23 and over the DBUF1 - DBUF8 bus. The Processor CCA, in turn, activates the TCVFU motor.

Each time the Processor CCA reads a TCVFU character off the tape, it stores it in the VFU portion of the line buffer within the Interface CCA.

When all TCVFU characters have been read once and stored, the Processor CCA performs another complete read operation. This time, each character read from the tape is compared against the same character stored during the first read operation. If all characters compare, the TCVFU load operation is complete. If a mismatch occurs in at least one character portion, a third read operation is performed and compared against the contents of the VFU memory stored during the second read operation. If necessary, a fourth or fifth read operation is performed until two successive read operations match. If no comparison is obtained within five read operations, the TCVFU load operation is aborted and the number 10 is displayed on the optional status display.

Unlike the loading of DAVFU characters, the printer must be off line while loading TCVFU characters, and while all handshaking operations are inactive.

### 2.4.2 Serial Interface CCA (Optional)

The Dataproducts Serial Interface CCA is designed to accept data from the user system in serial form, convert it to parallel form, and then to transfer the converted data to the Processor CCA. The following paragraphs describe the interface considerations between the Serial Interface CCA and the user system, the serial interface hardware, data management, and sequential operation.

#### a. Interface Considerations

Two types of serial data transmission can be accommodated by the Serial Interface CCA: RS232C, and 20 mA Current Loop. A selector switch within the Serial Interface CCA selects either type.

1. RS232C - In this type of serial interface, discrete voltage levels are used for transmitting data as well as for interface communication. A signal is ON or SPACING when its voltage level is more positive than +3V; a signal is OFF or MARKING when its voltage level is more negative than -3V. The data bits are low true.

2. 20-mA Current Loop - In this type of serial interface, data and communication signals are transmitted by means of two current loops: receive and transmit. The receive loop is made up of a two-wire (RxD+, RxD-) current source supplied by the user to the Serial Interface CCA. Within the Serial Interface CCA, the two wires of the receive current source are terminated in a current-sensing device.

The transmit current loop is controlled by the printer and terminated in a current-sensing device at the user end. Its purpose is to provide the user with printer status information. The presence of current in the transmit loop indicates that the printer is able to receive data. The absence of current in the transmit loop indicates that the printer is busy.

b. Interface Signals

Table 2-4 lists and defines the interface signals connected between the Serial Interface CCA and the user for both RS232C and current loop systems. Pin assignments are given for a standard 50-pin connector. Pin assignments for the optional 25-pin connector are given in section IV of the M120/M200 User's Guide, DPC 255174.

**TABLE 2-4. SERIAL INTERFACE 50-PIN AMP CONNECTOR PIN ASSIGNMENTS**

| Pin | Signal | Definition |
|---|---|---|
| 39 | (AB) | Signal Ground - This conductor establishes the common ground reference potential for all interface circuits. |
| 16 | (AA) | Protective Ground - This terminal can be connected to signal ground (AB) via a capacitor. |
| 22 | (BB) | Received Data - This user-generated signal transmits all print, format and control code information to the printer. This signal will only be looked at when the following signals are in the ON condition:<br><br>Data Terminal Ready<br>Data Set Ready (Optional)<br>Received Line Signal Detector (Optional) |
| 7 | (CD) | Data Terminal Ready - DTR - This printer-generated signal indicates that the printer is able to receive data. This signal is on when:<br><br>Printer power is on<br>No printer faults exist<br>Printer is on line<br>Printer buffer is not full<br><br>If the DTR signal goes off due to a PAPER OUT condition, it is possible that valid data may still be stored in the print buffer. In order to print the remaining data, paper must be reloaded and the on line mode re-entered via the ON LINE control panel switch. Any data remaining in the buffer will be printed and the printer will receive more data as soon as the DTR signal goes on. |
| 5, 3 | (BUSY) | Busy - This printer-generated signal is used to send status to the user. BUSY will be in the on condition whenever:<br><br>Data Terminal Ready is in the off condition.<br>The print buffer is more than 3/4 full. |

**TABLE 2-4. SERIAL INTERFACE 50-PIN AMP CONNECTOR PIN ASSIGNMENTS (Contd)**

| Pin | Signal | Definition |
|---|---|---|
| 5, 3 Contd | (BUSY) | Data loading can continue after the BUSY signal goes active; however, any data transmitted after the buffer is full will not be stored in the printer and the DTR signal will go off. |
| 27 | (RxD+) | Receive Data Plus - This user-generated signal transmits all print and control code information to the printer. This pin is positive with respect to (RxD-) when loop current is flowing (marking). This signal also indicates the status of the user equipment. Current is to be maintained in the loop, except while data is being transmitted, to indicate that the user equipment is in a ready condition. The absence of loop current for the period of one full transmission character will be interpreted by the printer as BREAK, indicating that the user equipment is not in a ready condition. |
| 11 | (RxD-) | Receive Data Minus - This signal is the current loop return for Receive Data. |
| 20 | (TxD+) | Transmit Data Plus - This printer-generated signal indicates that the printer is able to receive data. Current is allowed to flow in the transmit loop when:<br><br>Printer power is on<br>No printer fault exists<br>Printer has been placed on line<br>Print buffer is not full<br>Printer is not BUSY<br><br>This pin is positive with respect to (TxD-) when loop current is flowing (READY). |
| 4 | (TxD-) | Transmit Data Minus - This signal is the current loop return for Transmit Data. |
| 6 | (CC) | Data Set Ready - This user-generated signal indicates the status of the user equipment. The off condition of the DSR signal indicates that the printer must disregard signals on the other interface lines. The on condition indicates that the user equipment is in a ready condition. |

**TABLE 2-4. SERIAL INTERFACE 50-PIN AMP CONNECTOR PIN ASSIGNMENTS (Contd)**

| Pin | Signal | Definition |
|---|---|---|
| 23 | (CA) | Request to send - This printer-generated signal is held in the off condition to maintain the printer in the receive-only mode. |
| 8 | (CF) | Received Line Signal Detector - This user-generated signal, when in the on condition, indicates that the data communication equipment is receiving a signal (from the signal source) which meets its suitability criteria. These criteria are established by the data communication equipment manufacturer. |
| 9 | (CB) | Clear to Send - This user-generated signal indicates that the user system is ready to receive data. |
| 21 | (BA) | Transmitted Data - This printer-generated signal transmits control information to the user system. The printer cannot transmit unless an on condition is present on all the following signals:<br><br>(1) Request to Send (CA (2) Clear to Send (CB) (3) Data Set Ready (CC) (4) Data Terminal Ready (CD) |
| 24 | (CE) | Ring Indicator - This user-generated signal indicates that a ringing signal is being received by the printer. When this signal is in the on condition, it will activate the Data Terminal Ready line on the first ring. The printer must be powered up, ready, and on line. |

c. Hardware Description (Figure 2-11)

Figure 2-11 is a block diagram of the circuits which implement the Serial Interface CCA, including microprocessor chip U1. USART chip U29, input buffer U5-U17, print buffer U10-U11, and associated devices and logic circuits. The Serial Interface CCA performs three main functions:

Converts serial data of either the RS232C or Current Loop type into parallel form.

Processes and stores the converted data, and upon request, transfers it to the Processor CCA.

Channels, but does not process, data from the optional TCVFU reader and the option configuration switches to the Processor CCA.

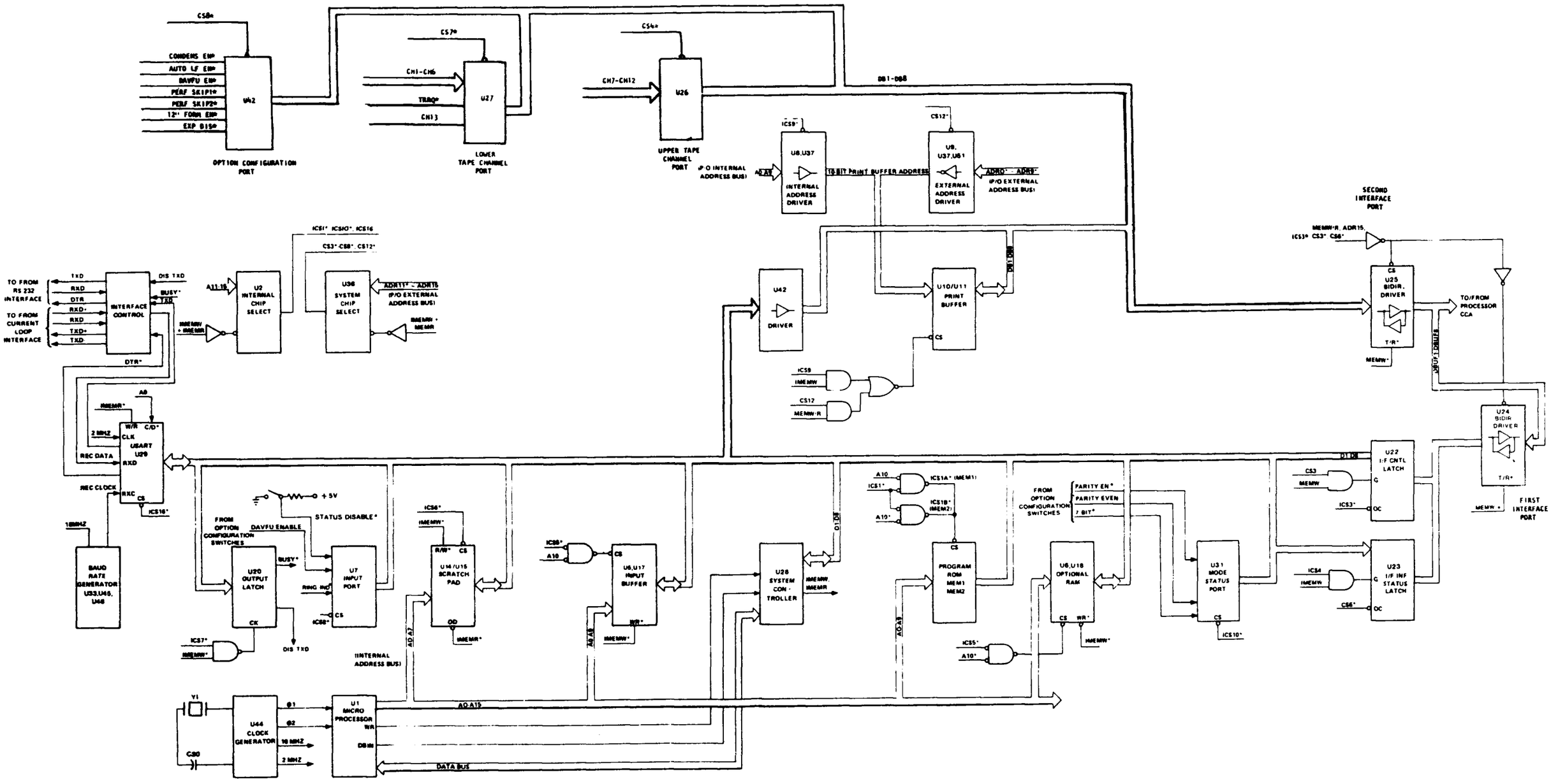



Figure 2-11. Serial Interface CCA Block Diagram

1. Control - Operation of the Serial Interface CCA is under control of two processors: internal, and external. The internal processor, hereafter referred to as the interface processor, is comprised of microprocessor chip U1, system controller chip U28, and clock generator chip U44. The external processor, hereafter referred to as the print processor, in general refers to the Processor CCA.

Each processor has an 8-bit data bus, an 16-bit address bus, and memory-write and memory-read control signals. Each 16 bit address bus is used to select a device from the complement of input/output devices connected to it and, where applicable, to specify the location within the selected device. The 8-bit data bus throughputs data between the applicable processor and the selected device. The memory-write and memory-read signals specify the direction of the data flow.

For example, when the print processor intends to transmit data to one of the devices within the Serial Interface CCA, it first places data on bus DBUF1-DBUF8. Then, it activates control signal MEMW, deactivates control signal MEMR, and places the address of the applicable device on address bus ADR0*-ADR15*. The procedure is similar when routing data from the Serial Interface CCA to the print processor, except that read control signal MEMR is activated, and write control signal MEMW is deactivated. Note that, when the print processor addresses the Serial Interface CCA (or any Interface CCA), address bit ADR15* must always be active.

Channeling data internally between the Interface Processor and one of the devices connected to it involves internal data bus D1-D8, internal address bus A0-A15, and internal read/write control signals IMEMR* and IMEMW*, with print processor address bit ADR15* inactive.

Table 2-5 lists the data bus, address bus, and control signals associated with each processor.

**TABLE 2-5. PROCESSOR I/O AND CONTROL SIGNALS**

| Processor | Data Signal | Address Signal | Control Signal |
|---|---|---|---|
| Interface (Internal) | D1 - D8 | A0 - A15 | IMEMW<br>IMEMR |
| Print (External) | DBUF1 - DBUF8 | ADR0* - ADR9*<br>ADR11* - ADR15*<br>(ADR10* not used) | MEMW*<br>MEMR* |

From the standpoint of control, the complement of devices within the Serial Interface CCA may be divided into three groups. One group of devices is under the exclusive control of the interface processor, while the second group of devices is under the exclusive control of the print processor. The third group of devices is accessible to either processor on a time-shared basis. Device control is effected by means of two sets of chip-select signals developed from the five (or six) most significant address bits of each processor. Chip select signals CS3* -CS8 * and CS12* are generated by external chip select decoder U36 from print processor address bits ADR11* - ADR15*. Similarly, chip select signals ICS1* - ICS10* and ICS16* are generated by internal chip select decoder U2 from interface processor address bits A11 - A15.

Another internal address bit, A10, is selectively used to distinguish between two devices that share a common chip select signal. External chip-select signals are listed in table 2-3. Signal CS12* is generated within the Serial Interface CCA by ORing CS1* with CS2*.

Table 2-6 lists the internal chip select signals and describes their functions.

**TABLE 2-6. INTERNAL CHIP SELECT SIGNALS**

| Signal | Binary Address | | | | | | Function |
|---|---|---|---|---|---|---|---|
| | A15 | A14 | A13 | A12 | A11 | A10 | |
| ICS1A* | 0 | 0 | 0 | 0 | 0 | 0 | Select Program ROM MEM1 |
| ICS1B* | 0 | 0 | 0 | 0 | 0 | 1 | Select Program ROM MEM2 |
| ICS3* | 0 | 0 | 0 | 1 | 0 | X | Select I/F Control Latch U22 |
| ICS4* | 0 | 0 | 0 | 1 | 1 | X | Select I/F Information. Latch U23 |
| ICS5A | 0 | 0 | 1 | 0 | 0 | 0 | Select Input Buffer U5/U17 |
| ICS5B* | 0 | 0 | 1 | 0 | 0 | 1 | Select Optional RAM U15, U5 |
| ICS6* | 0 | 0 | 1 | 0 | 1 | X | Select Scratch Pad Memory U15/U14 |
| ICS7* | 0 | 0 | 1 | 1 | 0 | X | Select Output Latch U27 |
| ICS8* | 0 | 0 | 1 | 1 | 1 | X | Select Input Port U7 |
| ICS9* | 0 | 1 | 0 | 0 | 0 | X | Select Print Buffer U10/U11 for internal write, together with internal buffer address driver U8, U37 |
| ICS10* | 0 | 1 | 0 | 0 | 1 | X | Select Mode Status Port U31 |
| ICS16* | 0 | 1 | 1 | 1 | 1 | X | Select USART U29 |

X = Don't care condition

2. Data Bus Structure and Device Description - There are a total of three data buses within the Serial Interface CCA: DBUF1 - DBUF8, DB1 - DB8, and D1 - D8. Bus DBUF1 - DBUF8 channels all data between the Serial Interface CCA and the Processor CCA. Two devices connect to bus DBUF1 - DBUF8: bidirectional drivers U25 and U24. Bidirectional driver U24, through devices U22 and U23 and bus D1 - D8, provides two-way communication between the Processor CCA and processor chip U1 of the Serial Interface CCA. Bidirectional driver U25 connects bus DBUF1 - DBUF8 to bus DB1-DB8, and allows the Processor CCA to access the print buffer U10/U11, as well as option configuration port U42, and tape channel ports U26 and U27. Latch U23 stores status information supplied by the Serial Interface CCA from data bus D1 - D8, under control of internal chip select signal ICS4* along with IMEMW. The contents of U23 are periodically sampled by the Processor CCA under control of external chip-select signal CS6*.

Latch U22 stores status and commands supplied by the Processor CCA under control of external chip-select signal CS3 along with MEMW. The contents of U22 are periodically sampled by the interface processor under control of internal chip-select signal ICS3*.

Since bus DBUF1 - DBUF8 is time-shared by U24 and U25, the two devices are enabled by a mutually exclusive arrangement: U25 is enabled by the expression MEMW/R.ADR15.ICS3*.CS3*.CS6*, where

MEMW/R.ADR15 = Processor CCA initiates an I/O read or write operation

ICS3*.CS3*.CS6* = Chip select signals controlling U22 and U23; U25 is disabled when any one of these signals is active

U25 is enabled under conditions opposite from U24, i.e., when either CS3*, CS6* or ICS3* is active.

Bus D1 - D8 serves as the bi-directional data path between the interface processor and the various memory and I/O devices connected to it. The function of each device is listed below:

(a) Input Port U7 - When selected by ICS8, this buffered port reads and inverts the state of the DAVFU ENABLE, and TCVFU ENABLE lines supplied by the option configuration switches. Bit designations are as follows:

| | | |
|---|---|---|
| MSB | D8 | RESET |
| | D7 | - |
| | D6 | - |
| | D5 | - |
| | D4 | RESET DELAYED |
| | D3 | DAVFU ENABLE* |
| | D2 | TCVFU ENABLE* |
| LSB | D1 | - |

(b) Output Latch U20 - This latched port stores various conditions of the Serial Interface CCA. It is updated by the interface processor with ICS7.IMEMW. Bit designations are as follows:

| | | |
|---|---|---|
| MSB | D8 | USART and BAUD rate generator reset |
| | D7 | - |
| | D6 | - |
| | D5 | - |
| | D4 | - |
| | D3 | - |
| | D2 | RLSD DLY RST |
| LSB | D1 | BUSY* |

(c) Scratch Pad U14 - U15 - This random access memory stores various flags, counters, status words, and pointers. It is selected by ICS6 on the interface word processor and is mapped as shown in table 2-7.

**TABLE 2-7. SCRATCH PAD MEMORY MAP**

| Location (Hex) | Contents |
|---|---|
| 2800 | OPST (Output Port Status) |
| 2801 | RBFLAG (Rest Busy Flag) |
| 2802 | LLCNT (Line Loaded Counter, LSB) |
| 2803 | LLCNTA (Line Loaded Counter, MSB) |
| 2804 | HLFLAG (Halt Flag) |
| 2805 | BSFLAG (Busy Flag) |
| 2806 | CMNDST (USART Command Word Status) |
| 2807 | LTFLAG (Line Transfer Flag) |
| 2808 | BLCNT (Buffer Length Counter) |
| 2809 | BOFLAG (Busy Off Line Flag) |
| 280A | HALTPT (Halt Pointer, LSB) |
| 280B | HALTA (Halt Pointer, MSB) |
| 280C | BUSYPT (Busy Pointer, LSB) |
| 280D | BUSYA (Busy Pointer, MSB) |
| 280E | BUFTOP (Input Buffer Top + 1, LSB) |

**TABLE 2-7. SCRATCH PAD MEMORY MAP (Contd)**

| Location (Hex) | Contents |
|---|---|
| 280F | BUFTPA (Input Buffer Top - 1, MSB) |
| 2810 | HLCNT (Halt Counter) |
| 2811 | COUNT1 (Counter #1) |
| 2812 | COUNT2 (Counter #2) |
| 2813 | TRLNST (Transfer Line Status Word) |
| 2814 | PTBST (Port B Status) |
| 2815 | DBLCNT (DAVFU Buffer Length Counter, LSB) |
| 2816 | DBLCTA (DAVFU Buffer Length Counter, MSB) |
| 2817 | DABPT (DAVFU Buffer Pointer, LSB) |
| 2818 | DABPTA (DAVFU Buffer Pointer, MSB) |
| 2819 | DAFLAG (DAVFU Flag) |
| 281A | DAFLT (DAVFU Fault Flag) |
| 281B | PBTAS (PBPT Temp. Store, LSB) |
| 281C | PBTASA (PBPT Temp. Store, LSB) |
| 281D | INTCH (Interim Character Received Counter) |
| 281E | XONFG (X-ON Only Once Flag) |
| 281F | XOFFG (X-OFF Only Once Flag) |
| 2820 | BSOFPT (Busy OFF Pointer, LSB) |
| 2821 | BSOFFA (Busy OFF Pointer, MSB) |
| 2822 | CRFGTR (Termination Flag) |
| 2823 | TERADD (Lower Address Byte) |
| 2824 | TERADD (Upper Address Byte) |
| 2826 | STATEG (Status On/Off Line Flag) |
| 2828 | NOPAR (Don't Care Parity Flag) |

(d) Input Buffer U17-U5 - This random access memory serves as a temporary storage device for all print and control characters supplied by the user system and converted by USART chip U29. It is accessed under control of signal ICS5 when A10 is inactive.

(e) Program PROM MEM1-MEM2 - PROMs MEM1 and MEM2 store the main program for the interface processor and are accessed under control of internal chip-select signals ICS1A and ICS1B.

(f) Optional RAM U18-U6 - This device is an optional extension of input buffer U17-U5, under control of signal ICS5 with bit A10 active.

(g) Mode Status Port U31 - This device defines the operating parameters of the USART chip, such as number of stop bits, type of parity, if any, character length, and BAUD rate. Input to this device is supplied in part by the Option Configuration switches and selected in part by parameter switches within the Serial Interface CCA. It is accessed under control of internal chip-select signal ICS10, and has the following bit assignments:

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MSB | D8 | Number of | D8 | 0 | 0 | 1 | 1 |
| | D7 | Stop Bits | D7 | 0 | 1 | 0 | 1 |
| | | | Stop Bits | X | 1 | 1½ | 2 |
| | D6 | Even Parity | | | | | |
| | D5 | Parity Enable | | | | | |
| | D4 | Character | D4 | 0 | 0 | 1 | 1 |
| | D3 | Length | D3 | 0 | 1 | 0 | 1 |
| | | | No. Bits | 5 | 6 | 7 | 8 |
| | D2 | Baud Rate | D2 | 0 | 0 | 1 | 1 |
| LSB | D1 | Factor | D1 | 0 | 1 | 0 | 1 |
| | | | Factor | SYNC | X1 | X16 | X64 |

(h) USART Chip U29 - In its application as a component of the Serial Interface CCA, USART chip U29 is used mainly as an asynchronous receiver. Operating under control of internal chip-select signal ICS16, along with IMEMW and IMEMR, it converts the serial bit stream into parallel characters, inserting or deleting bits as required by the communications technique used. In addition to converting serial data into parallel form, U29 tests each character for parity (if applicable), overrun, and frame errors. If an error condition is detected, it is reported when interrogated by the interface processor. Inputs to U29 include signals REC DATA, REC CLOCK, and 2mHz CLOCK. Signal REC DATA is a gated version of the serial data stream supplied by the user system and processed by the interface control circuits. Signal REC CLOCK is supplied by the BAUD rate generator, and is used to synchronize U29 with the BAUD rate of the serial data stream. Signal 2mHz serves as a time base for internal device timing. Output signal DTR indicates that the printer is able to receive data.

generator, and is used to synchronize U29 with the BAUD rate of the serial data stream. Signal 2mHz serves as a time base for internal device timing. Output signal DTR indicates that the printer is able to receive data.

When operating as an asynchronous transmitter, the USART chip receives data in parallel format from processor chip U1 on D1-D8, and transmits the data in a serial bit stream to the user. Information transmitted in this fashion includes status words X-ON and X-OFF.

Communications between the USART chip and the interface processor are performed over data bus D1-D8 under control of signals C/D*, RD*, WR* in one of three modes, as follows:

(1) Data Transfer Mode: C/D* = O, RD* = 0, WR* = 1

| | | |
|---|---|---|
| LSB: | D1 | |
| | D2 | Parallel data |
| | D3 | word transferred |
| | D4 | from USART to |
| | D5 | the interface |
| | D6 | processor |
| | D7 | |
| MSB: | D8 | |

(2) Status Mode: C/D* = 1, RD* = 0, WR* = 1

| | | | |
|---|---|---|---|
| LSB: | D1 | = Transmitter Ready | |
| | D2 | = Receiver Ready | Status word |
| | D3 | = Transmitter Empty | from USART |
| | D4 | = Parity Error | to the |
| | D5 | = Overrun Error | interface |
| | D6 | = Framing Error | processor |
| | D7 | = Sync Detect | |
| MSB: | D8 | = Data Set Ready | |

(3) Command Mode: C/D* = 1, RD* 1= 1, WR* = 0

| | | | |
|---|---|---|---|
| LSB: | D1 | = Transmit Enable | |
| | D2 | = Data Terminal Ready | Command |
| | D3 | = Receive Enable | word from |
| | D4 | = Send Break Character | interface |
| | D5 | = Error Reset | processor |
| | D6 | = Request to Send | to USART |
| | D7 | = Internal Reset | |
| MSB | D8 | = Sync | |

(i) BAUD Rate Generator U33-U45-U46 - This circuit group supplies the receive and transmit clock signals to USART chip U29. Input to the BAUD rate generator is the 18mHz clock supplied by the interface processor. With BAUD rate select switch S3 set to the desired BAUD rate, the frequency of the output clock is 16 times the expected BAUD rate of the serial data.

(j) Interface Control - This circuit group controls communication and data flow between the user system and the USART chip U29. The user system may be either the RS232C or 20 mA current loop type. With either type of system, the interface control presents a uniform interface to USART chip U29.

The main output from the interface control to the USART chip U29 is serial data signal REC DATA. This signal is derived either from the RxD input signal of the RS232 type interface, or from the current variation in the RxD+/RxD- receive loop, as applicable. Output to the RS232C interface includes signals DTR and BUSY. Signal DTR is derived from DTR* supplied by the USART chip U29. Signal BUSY is derived from BUSY* obtained from output port U20. When the interface is a 20-mA current loop type, the TxD+/TxD- transmit loop is used to transmit the BUSY status; a BUSY condition is signified by an absence of current flow in the TxD+/TxD- loop.

(k) Print Buffer U10/U11 - The print buffer is accessible to both internal processor chip U1 and the external processor located in the Processor CCA. Typically, internal processor chip U1 stores user data in the print buffer, such as print and paper motion characters and DAVFU tape channel information. Note that processor chip U1 only writes information into the print buffer, but does not read its contents.

As an example, assume that processor chip U1 intends to write a print character at a given location in the print buffer. To do this, U1 places the ASCII-coded character on bus D1-D18, activates, through U2, internal chip select signal ICS9*, and internal write signal IMEMW. With ICS9* active, ASCII driver U21 is enabled, and the contents of D1-D8 are channelled to the print buffer on bus DB1-DB8. ICS9* also enables internal address driver U8/U37, allowing U1 to specify the location address where the character is to be stored. Then IMEMW is raised, and the contents of DB1-DB8 are loaded into the selected location of the print buffer.

The Processor CCA can both read the contents of or write into the print buffer. Typically, the Processor CCA will read the contents of the print buffer to obtain the print and paper motion characters originally supplied by the user, or VFU tape channel information supplied either by the user or obtained from the paper tape. To do this, the Processor CCA codes the address bits that generate chip select signal CS12*, and with bit ADR15 active, enables bi-directional driver U25 and external address drivers U9, U37, and U51. When MEMR is activated, the expression CS12*. MEMW/R enables the print buffer, and its contents are read by the Processor CCA on bus DB1 - DB8.

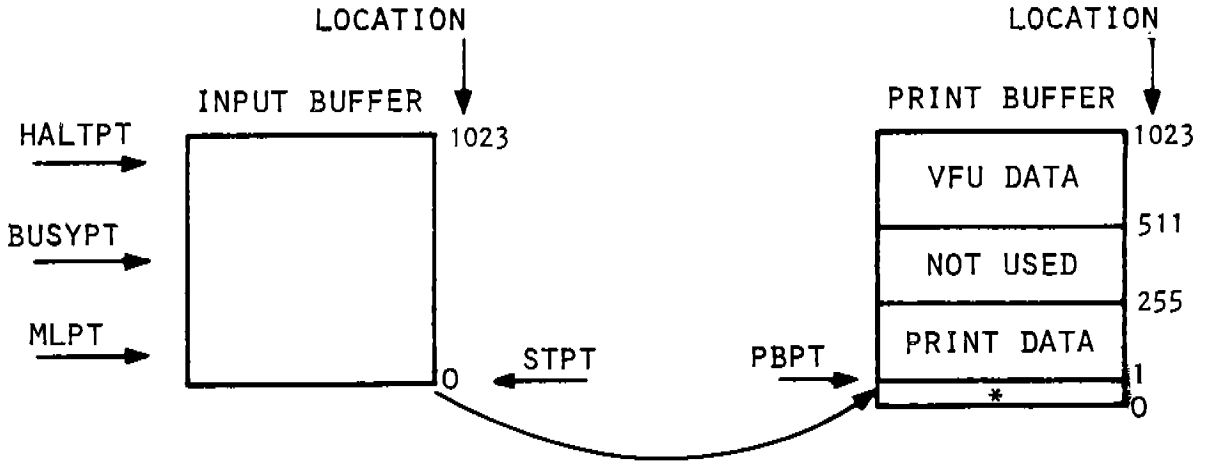
In the write mode, the Processor CCA typically writes tape channel information obtained from the TCVFU into the upper half of the line buffer. The procedure is similar to the read operation described above, except that signal MEMW replaces MEMR, thus reversing the direction of data flow through U25. Note that tape channel information originating in the TCVFU is first read by the Processor CCA, and then written into the print buffer one character at a time. This operation is performed while the printer is still off line. When in the off line mode the printer receives a VFU-type paper instruction from the user. The Processor CCA reads the contents of the print buffer to obtain the format, and accordingly, executes the paper instruction.

d. Data Management (Figure 2-11)

Two buffer memories are incorporated in the Serial Interface CCA: input buffer U5/U17, and print buffer U10/U11. The input buffer stores, in a circular fashion, all print and control characters received from the user system, line after line. Upon request by the print processor, one complete line is transferred to the print buffer, one character at a time. When the transfer is completed, the print processor examines the contents of the print buffer and eventually prints it. Line transfer is initiated when the print processor sets the load buffer signal. This signal is latched in bit D3 of the interface control latch U22. When the transfer is completed, the interface processor informs the print processor by latching signal BUFFER FULL in bit D1 of the interface information latch U23. In response, the print processor resets the LOAD BUFFER signal and then the interface processor resets the BUFFER FULL signal. Note that the LOAD BUFFER and BUFFER FULL signals operate in a handshaking fashion.

Therefore, there are two major operations taking place in the Serial Interface CCA: loading the input buffer with user-supplied data, and transferring complete lines to the print buffer. A third operation, involving DAVFU data, is treated in a special way and is discussed in paragraph 2.3.2. Note that the transfer of data from the print buffer to the print processor is an operation involving the print processor but not the interface processor.

To keep track of the buffer status and preserve the integrity of the data, the interface processor maintains a group of pointers, counters, and flags in designated locations within the scratch pad buffer U14/U15. Following initialization, all pointers are reset to the status shown in figure 2-12. The main loop pointer (MLPT) points to the location where the next user-supplied character is to be loaded in the input buffer, in this case, location 0. Start transfer pointer (STPT) points to the first character location of the next complete line to be transferred to the print buffer, in this case location 0. Starting from zero, the line length counter (LLCT) increments with each complete line received from the user, and decrements with each complete line transferred to the print buffer. The print buffer pointer (PBPT) points to the location in the print buffer where the next character is to be stored and increments with each transferred character. BUSY pointer (BUSYPT) points to the address where the input buffer is 3/4 full. The halt pointer (HALPT) points to the top location of the input buffer.




* LOCATION 0 IS RESERVED FOR LOCATION ADDRESS OF THE CONTROL CHARACTER

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Figure 2-12. Buffer Pointers

1. USART to Input Buffer Data Transfer - Figure 2-13 shows the data structure of the input buffer. When a character is received from the USART, it is stored at the location pointed to by main loop pointer MLPT. Since MLPT initially always points to the start of the buffer, the first print character received from the USART is always stored at the start or bottom of the buffer. With each character received from the USART, MLPT is incremented.

Subsequent print characters are treated the same way, each stored sequentially in the next highest location. Receipt of a control character (paper motion) marks the end of that print line. The control character is stored above the last print character, MLPT is incremented by one, and a dummy character ($IF_H$) is stored one location above the control character. The dummy character serves as a demarcation for each print line. Next, a transfer line status code is stored one location above the control character. The transfer line status code contains the horizontal pitch (normal, condensed, or expanded) of the current line. Transfer line status information is derived from a coded character supplied by the user at any time, but is not loaded in the input buffer until the line has been terminated. Finally, the lines loaded counter (LLCNT) is incremented to indicate that one complete line is ready to be transferred to the print buffer.

To circulate the input buffer, the main loop pointer is continually compared with the top-of-buffer pointer (BUFTOP). If BUFTOP is one location higher than the physical top of the input buffer, the main loop pointer is returned to the physical bottom address of the input buffer.

To avoid overfilling the input buffer, the main loop pointer is continually compared to the busy pointer BUSYTP. When the two are equal, indicating that the input buffer is 3/4 full, a BUSY signal is sent to the user system. Under these circumstances, the user is allowed to complete transmission of the current line, then stop until the BUSY condition is lifted. If the user ignores BUSY and keeps transmitting, the input buffer will eventually fill up, and the HALT flag will be set. With the HALT flag set, the interface control circuit will disable Data Terminal Ready signal DTR, and any further data will be ignored until the BUSY condition is lifted. The BUSY condition will be lifted when enough data has been transferred to the print buffer to make the input buffer less than 1/4 full.

2. Input Buffer to Print Buffer - This operation involves the transfer of one line of data, character by character, from the input buffer to the print buffer. One line of data includes print data and the control character, but not the dummy character or the transfer line status character. The source of the first character to be transferred is the location address pointed to by the start transfer pointer STPT. The destination of the first character to be transferred is the location address pointed to by the print buffer pointer PBPT. Both pointers are incremented with each transferred character.

The operation is initiated when the print processor sets control signal LOAD buffer in bit D1 of interface control latch U22. With bit D1 set, the transfer operation can start if the line length counter is greater than zero. Before a character is transferred, it is first compared with the dummy character. If it is not a dummy character, then it is stored in the designated location within the

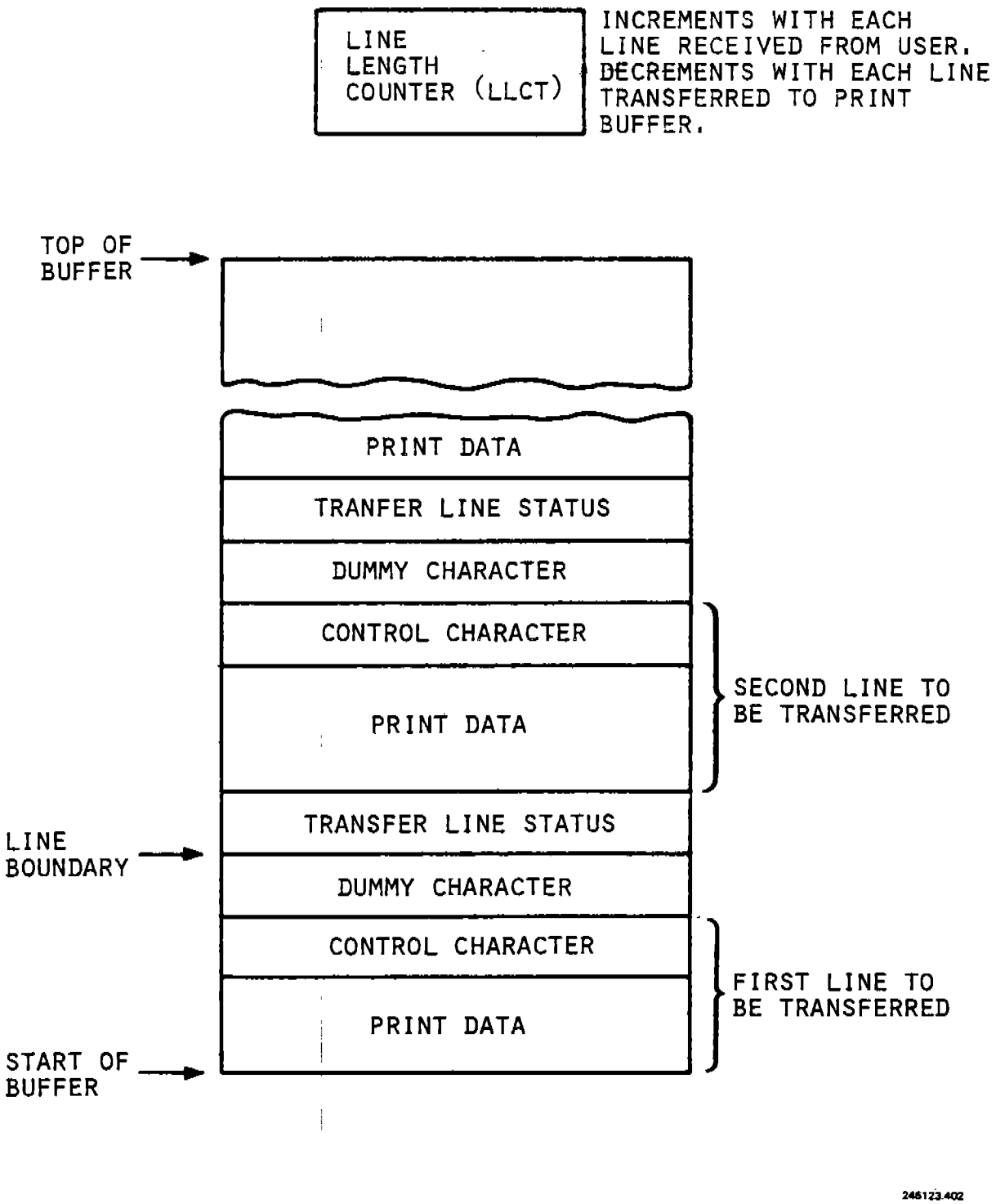



Figure 2-13. Input Buffer Structure

print buffer. Following transfer of each non-dummy character, the USART chip is interrogated. Interrogation of the USART chip involves testing for the presence of a newly assembled character, and if applicable, storing that character in the designated location within the input buffer.

When the dummy character is detected, the location address of the control character is stored in location 0 of the print buffer. Next, the contents of the transfer line status is examined to determine if the line pitch is expanded, condensed, or normal. This information, along with the BUFFER FULL signal, is sent via the interface information latch U23 to the print processor.

Each time a character is transferred to the print buffer, the memory space in the input buffer increases. Accordingly, the BUSYPT (input buffer 3/4 full) and HALTPT are incremented. When a complete line has been transferred to the print buffer, the conditions of the HALT flag (HLFLAG) and 3/4 BUSY flag (BSFLAG) are reexamined. If either flag is set, and the input buffer is less than 1/4 full, both flags are reset, and the BUSY signal to the user system is deactivated.

In addition, when transferring characters from the input buffer to the print buffer, the input buffer pointers are checked against the value of BUFTOP. If either the start transfer pointer, BUSY pointer, or HALT pointer, equals BUFTOP, it is reinitialized to the physical bottom of the input buffer. This allows the input buffer to operate in a circular fashion.

3. DAVFU Data Transfer - Unlike print data, DAVFU data is not loaded first in the input buffer, but is transferred directly from the USART chip to the VFU portion of the print buffer. When a DAVFU start code is received, the BUSY signal to the user is activated and DTR is deactivated. Next, the contents of the input buffer, if any, are transferred to the print buffer. Once the input buffer is completely empty, DTR is activated again and BUSY is deactivated. Upon receipt of a LOAD BUFFER signal from the print processor, loading of DAVFU data may then be resumed.

DAVFU loading operations are terminated upon one of the following conditions:

(a) When a DAVFU load error is detected. Under this condition, the interface processor will transmit a DAVFU FAULT signal on bit D3 of the interface information latch U23 to the print processor.

(b) When a DAVFU start character is received from the user system. This condition will restart the DAVFU load operation.

(c) When a DAVFU stop character is received and no error conditions exist. Following a successful DAVFU load operation, the location address of the last DAVFU character is stored in location 0 of the print data portion of the print buffer.

4. Sequential Operation - The following paragraphs describe, in simplified form, the sequence of events associated with the transfer of data from the USART chip through the input buffer to the print buffer. The discussion is divided into the following topics, each keyed to a flow diagram:

Overall Operation

Input Operation

Print Data Transfer Operation

DAVFU Data Transfer Operation

(a) Overall Operation (Figure 2-14) - Figure 2-14 is a general flow diagram of events associated with the operation of the Serial Interface CCA. Following initialization, the ON LINE signal is monitored; the Serial Interface will remain in this loop until the print processor enters the on-line state. As part of this loop, the USART is monitored for the presence of a status request character supplied by the user. If a status request character is detected, the status check (STACK) operation is entered, and the status request is serviced.

When the ON LINE signal goes high, the serial interface returns an on line ACKNOWLEDGE signal to the print processor and clears BOFLAG (BUSY flag set when the processor goes off line). Next, the conditions of DAFLAG (set following receipt of a DAVFU start code) and BSFLAG (set when the input buffer is 3/4 full) are tested. If neither flag is set, the BUSY signal to the user system is reset, DTR (Data Terminal Ready) is enabled, and an X-ON operation is performed.

NOTE

The serial interface will go BUSY and activate the BUSY signal to the user under any of the following conditions:

When the print processor goes off line, and will stay BUSY until the print processor goes on line again.

When the input buffer is 3/4 full, and will stay BUSY until enough data has been transferred to the print buffer to make the input buffer less than 1/4 full.

When a DAVFU start code has been received. The serial interface will stay BUSY long enough to allow transfer of all print data from the input buffer.

Next, the USART chip is examined for the presence of an assembled character. If a character is found to be present, it is stored in the input buffer. Otherwise, the ON LINE signal is monitored to verify that the print processor is still on line. Assuming that the ON LINE signal is still high, and that the print processor has set the LOAD BUFFER signal, the contents of the line loaded counter LLCNT is examined. If LLCNT does not equal zero, one line of data is transferred from the input buffer to the print buffer.

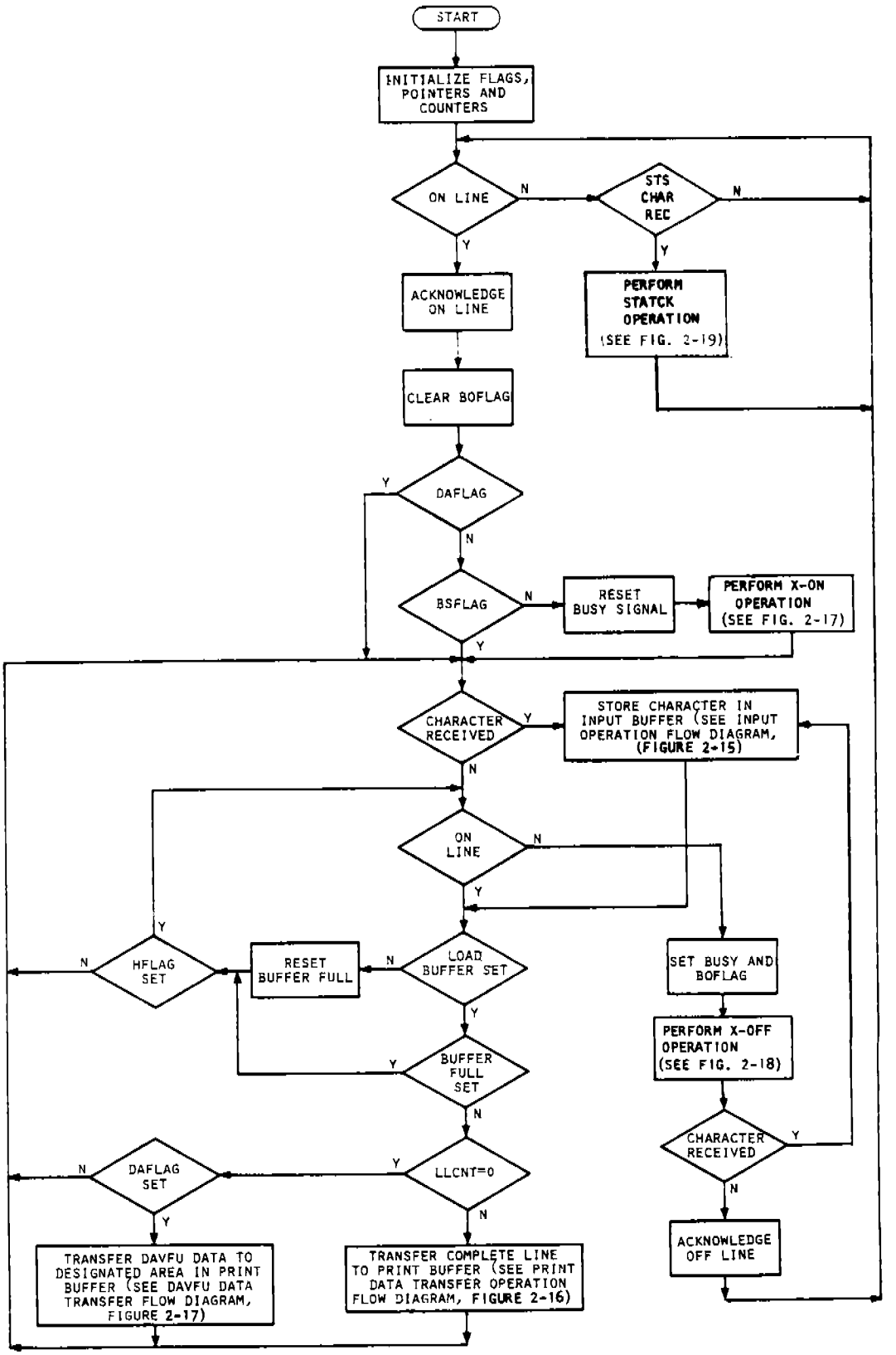



Figure 2-14. Serial Interface Overall Operation Flow Diagram

If the ON LINE signal is low, the BUSY signal to the user is activated, BOFLAG (BUSY due to off line) is set and an X-OFF operation is performed. See paragraph 2.4.2, subparagraph 1, for status transmission details. The BUSY signal informs the user to complete loading the current line, and then wait until the BUSY condition has been lifted. Next, the USART chip is tested for the presence of an assembled character. If a character is present, it is loaded in the input buffer. This operation is repeated several times until the user has completed transmitting the current line. At that time, the off-line signal is acknowledged, and the sequence returns to the on line signal monitoring loop.

Unlike print data, DAVFU data is transferred directly from the USART chip to the VFU portion of the print buffer. However, before DAVFU data can be serviced, the input buffer must be empty. To accomplish this, the contents of the input buffer are transferred, character by character, line after line, and printed. During this time, the BUSY signal is active and no characters are accepted from the user system. Each time a line is transferred from the input buffer to the print buffer, LLCNT is decremented by one. Eventually LLCNT will equal zero and the last line will be printed, allowing the serial interface to enter the DAVFU data transfer operation.

If, as a result of an input operation, HLFLAG is found to be in the set state, no input operation can take place. Instead, the transfer operation is entered as many times as necessary until enough data has been transferred to allow HLFLAG to be reset.

(b) Input Operation (Figure 2-15) - During each input operation, one character is transferred from the USART to the input buffer. Each character is tested for load errors, control codes, and DAVFU start codes. No character loading can take place if the input buffer is already filled to capacity.

At the start of the input operation, the state of HALT flag HLFLAG is examined. If set, HLCNT is tested. If HLCNT equals 2, the input operation is exited and returned to the overall operation. Otherwise, HLCNT is incremented by one. If HLFLAG is not set, HLCNT is neither examined nor incremented.

NOTE

HLFLAG is set when all but two locations of the input buffer are full.

Next, the character supplied by the user through the USART is tested for framing, overrun, parity errors, and status request. If a framing or overrun is detected, a question mark (?) is stored. If the character is a status request, a status check (STCK) operation is performed. If a parity error is detected, a dollar sign ($) is stored. Otherwise, the character is stored unaltered in the input buffer and tested for the following:

(1) Print character.

(2) DAVFU start code. If present, DAFLAG and BUSY are set and DTR is reset, and an X-OFF operation is performed.

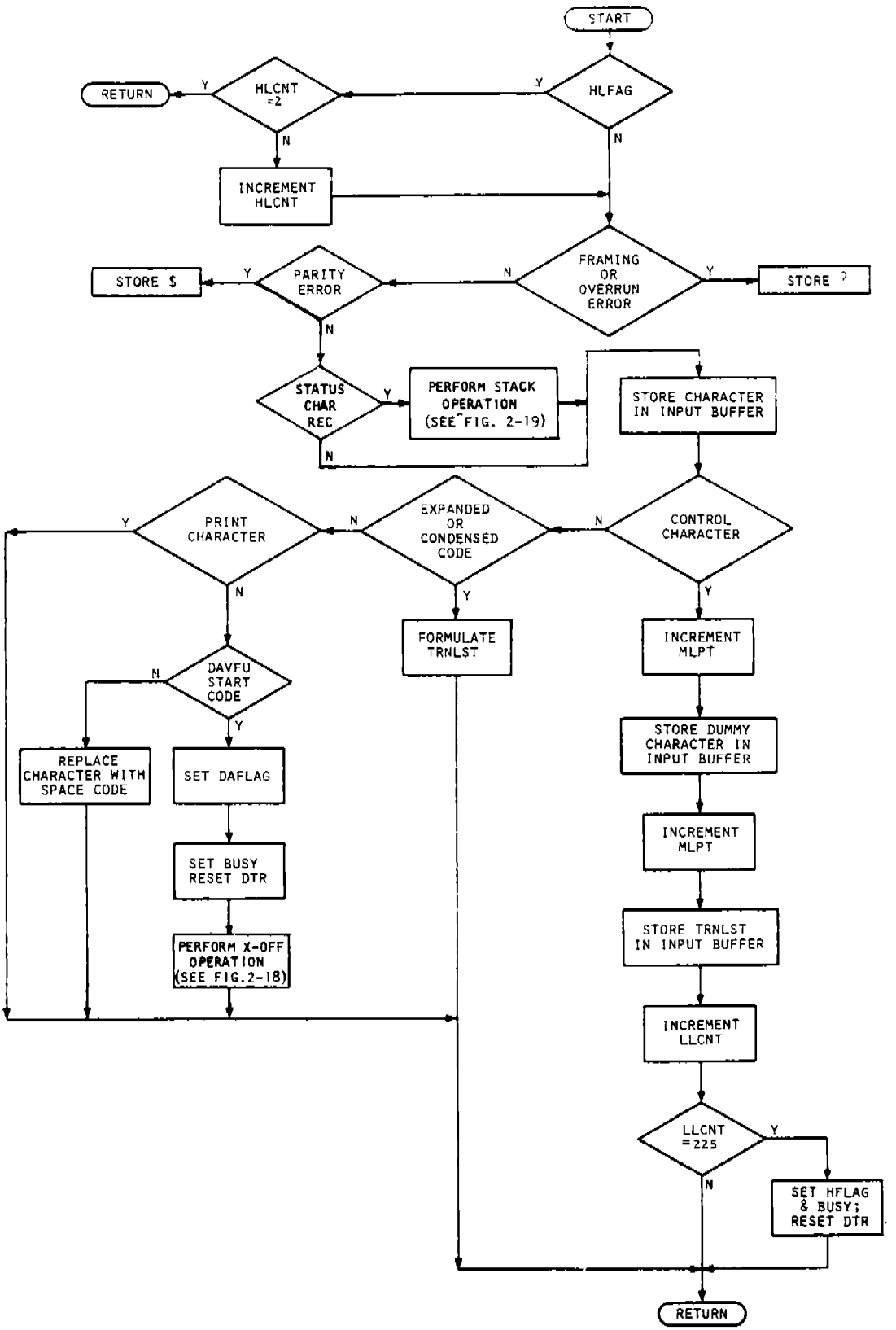



Figure 2-15. Input Operation Flow Diagram

(3) Control code. If present, the dummy character is stored above the control character, followed by TRNLST. After TRNLST has been stored, LLCNT is incremented and tested. If less than 255, the input operation returns to the overall operation. If LLCNT equals 255, indicating that the input buffer is now filled to capacity, HFLAG and BUSY are set, and DTR is reset before the input operation sequence is exited.

(4) Condensed or expanded code. If present, TRNLST is formulated accordingly.

(5) If none of the above is present, the character currently stored in the input buffer is replaced by a space code.

(c) Print Data Transfer Operation (Figure 2-16) - This operation transfers complete lines of print data, character by character, to the print buffer. Starting with location 1, characters are transferred one at a time in a continuous loop until one of the following two conditions are encountered:

(1) The USART needs to be serviced. Under this condition, the print data transfer operation is exited, and eventually the input operation is entered. During the input operation, the USART character is loaded in the input buffer, and then the print data transfer operation is reentered.

(2) A dummy character is detected indicating the end of the current line. Under this condition, the location address of the previous character (control character) is stored in location zero of the print buffer.

Next, interface information latch U17 is updated with the latest TRNLST status (condensed, expanded), and LLCNT is decremented. Finally, BUSY and HLTFLAG are reset, and DTR is set.

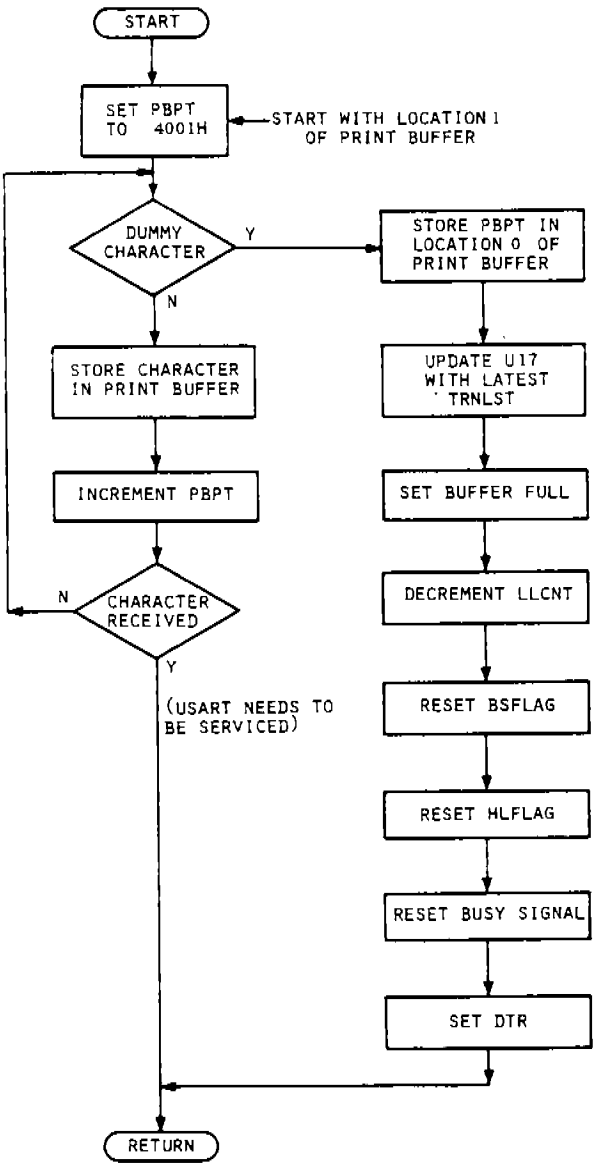
(d) DAVFU Data Transfer Operation (Figure 2-17) - During this operation, DAVFU data is transferred directly from the USART to the VFU area of the print buffer. Loading will proceed sequentially until one of the following occurs:

Receipt of another DAVFU start code.

DAVFU fault.

Receipt of a DAVFU stop code.

As shown in figure 2-17, the DAVFU fault flag, DAVFU Flag and BUSY signal are cleared, and DTR is set. Next, the operation enters a loop until the USART indicates that it has a character available for transfer. At that time, the character is tested for load error and DAVFU start code. Assuming that neither condition exists, the character is stored in the DAVFU area of the print buffer, in a location specified by the DAVFU buffer pointer DABPT. Next, the DAVFU character count is monitored for 511. Assuming that the count is less than 511, DAVFU character length counter DBLCNT and buffer pointer DABPT are incremented, and the character is tested for a DAVFU stop code. If the character is not a stop code, the operation returns to the USART monitoring loop until another character becomes available.




245123 408

Figure 2-16. Print Data Transfer Operation Flow Diagram

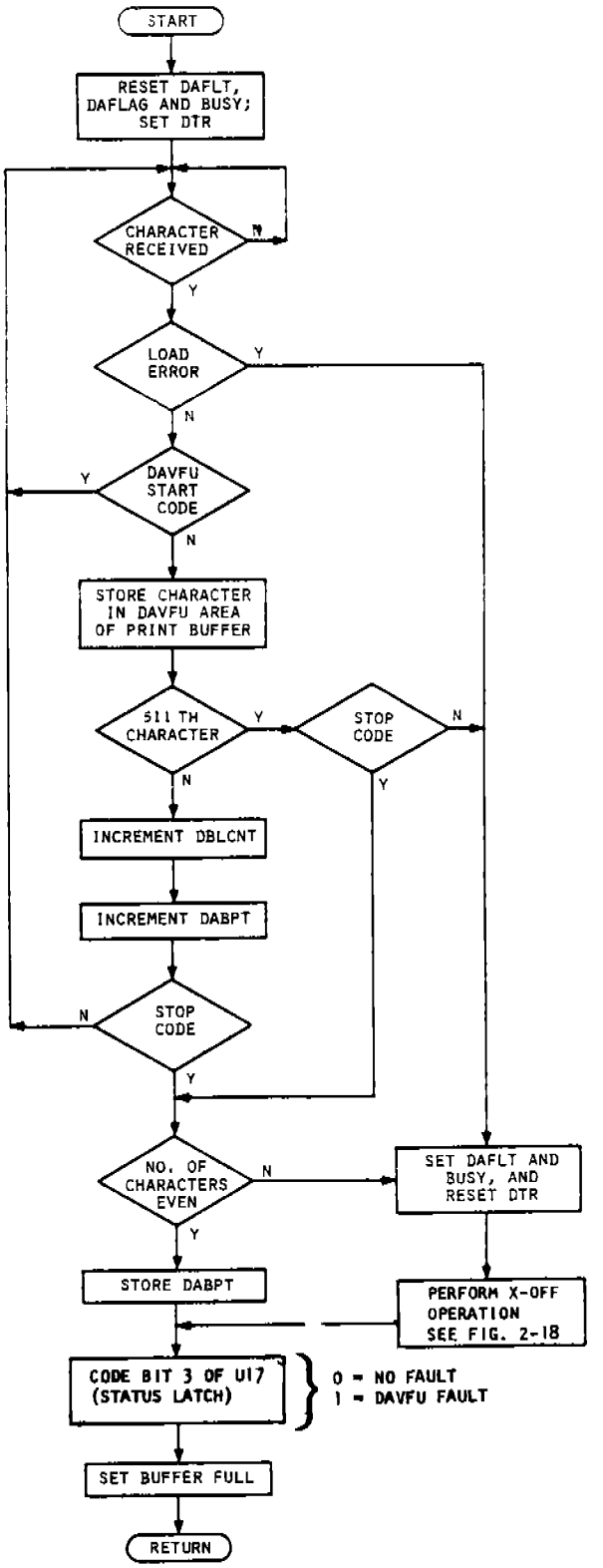



Figure 2-17. DAVFU Data Transfer Flow Diagram

Eventually, after receipt of several characters, the user will transmit a DAVFU stop code. If the number of DAVFU characters is even, DABPT is stored in location 0 of the print buffer; DAVFU fault bit D3 is coded in U17, (since no fault has occurred, D3 is set to 0); and BUFFER FULL is set in bit D1 of U17.

DAVFU fault can occur under the following conditions:

(1) Character load error.

(2) Number of characters equals 511, and no stop code was received.

(3) The total number of characters received, including the start and stop codes, is odd.

When a DAVFU fault occurs, DAFLT and BUSY are set, and DTR is reset. Then a DAVFU fault condition is reported to the print processor by setting bit D3 of U17 to one.

e. Status Transmission

In addition to receiving and processing user data, the Serial Interface CCA also transmits coded status information to the user. There are a total of five coded status words, arranged in two groups. One group of coded status words X=ON/X=OFF, is transmitted once each time the printer changes from BUSY to NOT BUSY to BUSY, respectively. The other group of status words, ACK, NAK, DC4, and X-OFF, is transmitted upon special request by the user. Note that status word X-OFF appears in both groups; i.e. X-OFF is transmitted automatically once when the status changes from NOT BUSY to BUSY, but may be transmitted again when requested by the user, provided that the printer is still in the BUSY state. Following is a detailed description of the status words in each group:

1. Group 1 - Prerequisite: The printer must be on line.

   X-ON

   Octal Code: 21

   Transmitted: Once, when the printer state changes from BUSY to NOT BUSY.

   X-OFF

   OCTAL Code: 23

   Transmitted: Once when the printer state changes from NOT BUSY to BUSY.

2. Group 2 - Prerequisite: Switch SW1-2 on the Serial Interface CCA must be set to OFF (status enabled). Once this condition is met, the printer will respond to a status request word (octal 5) provided by the user by transmitting any one of the following:

NAK

Octal Code: 25

Status: Printer is off line, and no faults exist.

DC4

Octal Code: 24

Status: Printer is off line, and a fault exists.

ACK

Octal Code: 6

Status: Printer is on line, and buffer is not full.

X-OFF

Octal Code: 23

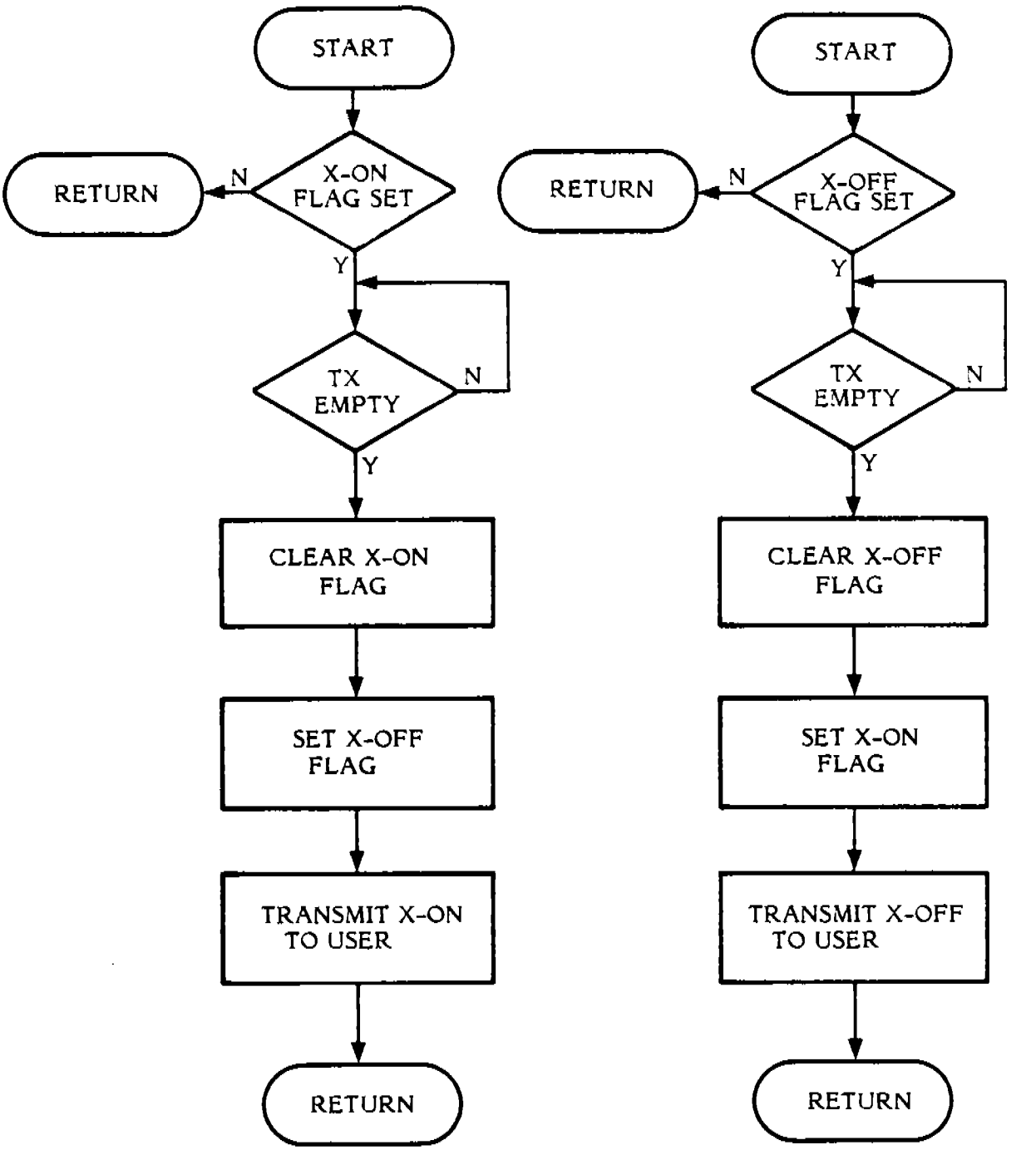
Status: Printer is on line and buffer is full.

NOTE

With Switch SW1-2 set to ON, receipt of a status request word (octal 5) will cause the printer to print a space.

Figures 2-18 and 2-19 show, in simplified form, the events associated with the X-ON, X-OFF, and status check operations. Operations X-ON and X-OFF are subroutines that may be entered from any other operation, provided that the printer is on line, and when the printer changes from BUSY to NOT BUSY or from NOT BUSY to BUSY. Typically, X-ON is entered following initialization when the printer goes on line and is not busy (see figure 2-14). Typically, X-OFF is entered from the overall operation, input operation, or DAVFU operation when the printer goes from NOT BUSY to BUSY.

Status check operation is a subroutine entered any time the user transmits a status request word (octal 5). Typically, it is entered from the overall operation while the printer is still off line (see figure 2-14), and from the input operation (see figure 2-15) when the printer is on line.




A. X-ON OPERATION

B. X-OFF OPERATION

Figure 2-18. X-ON/X-OFF Operation Flow Diagram

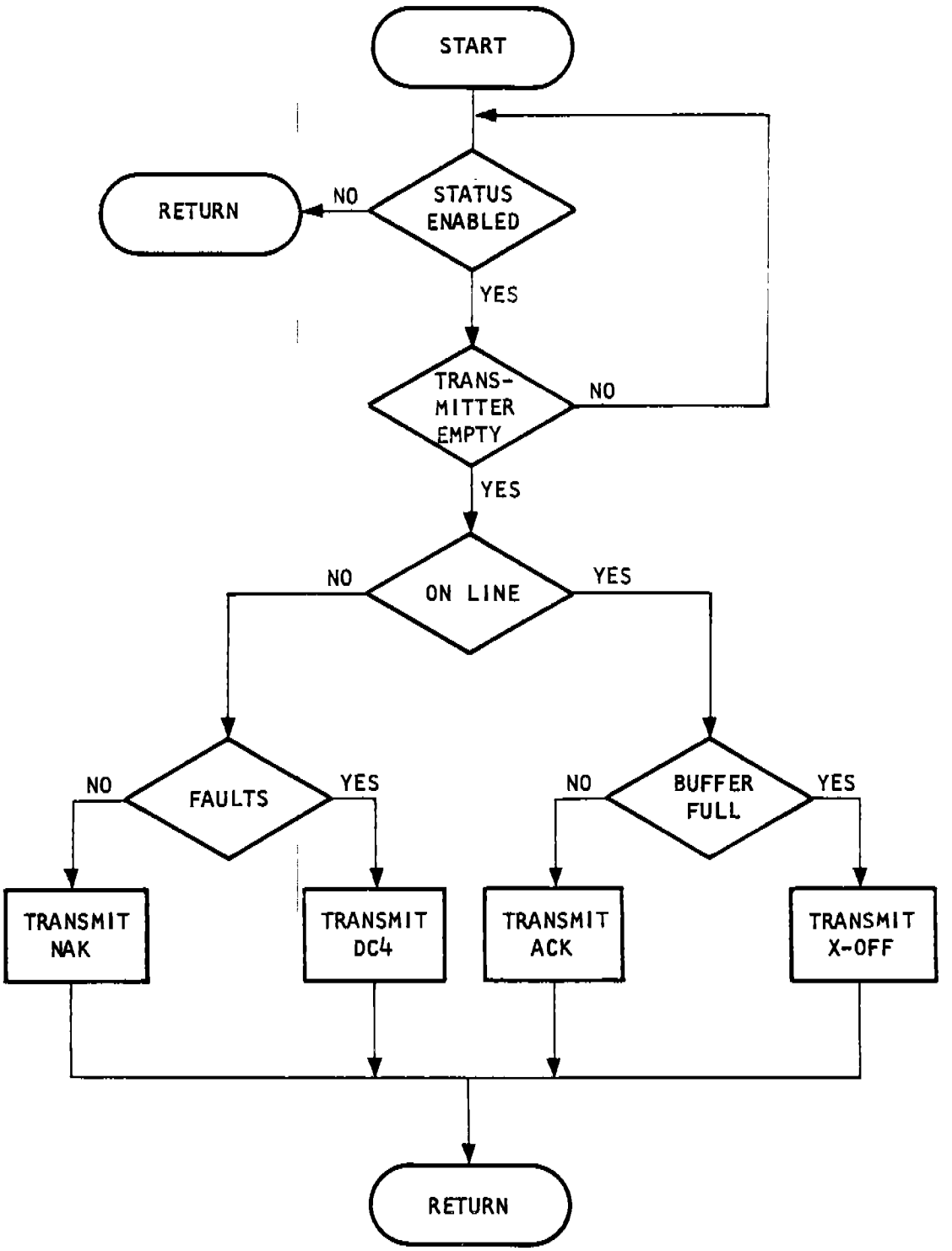



Figure 2-19. Status Check Operation Flow Diagram

f. Definition of Flags, Pointers, and Counters

Table 2-8 is an alphabetical list of flags, pointers, and counters used by the interface processor to transfer data from the USART to the print processor.

TABLE 2-8. DEFINITION OF FLAGS, POINTERS, AND COUNTERS

| Item | Definition |
|---|---|
| BLCNT | Buffer Length Counter. This counter records the number of characters loaded from the user to the Input Buffer for each line of data. |
| BOFLAG | Busy Off Line Flag. This flag is set to distinguish between a 3/4 full busy condition and a busy off line condition. It is set whenever the printer is put off line. Once set, the BUSY signal will not get reset unless the printer is again placed on line. |
| BSFLAG | Busy Flag. This flag is set when the Input Buffer is half full. |
| BSOFPT | Busy Off Pointer. This flag is set when the Input Buffer is down to 1/4 full. |
| BUFTOP (LSB), BUFTPA (MSB) | Input Buffer Top + 1. This is the address of the top location of the Input Buffer + 1. |
| BUSYPT (LSB), BUSYA (MSB) | Busy Pointer. This address pointer is 3/4 up the Input Buffer (with reference to the bottom of the next line to be transferred). It is used to set the Busy Flag when the Input Buffer is 3/4 full. |
| CMNDST | USART Command Word Status. This records the last command word written to the USART. |
| CRFGTR | Carriage Return/Terminator Flag. MSB set when previous line was terminated with a CR. LSB set when previous line was terminated with LF, FF, or VFU-type paper motion command. |
| DABPT (LSB), DABPTA (MSB) | DAVFU Buffer Pointer. Points to buffer memory address where the next DAVFU character is to be located. |

TABLE 2-8. DEFINITION OF FLAGS, POINTERS, AND COUNTERS (Contd)

| Item | Definition |
|---|---|
| DAFLAG | DAVFU Flag. This flag is set when a DAVFU start code is received from the user. |
| DAFLT | DAVFU Fault Flag. This flag is set if:<br>1. A DAVFU load error was detected.<br>2. DAVFU Buffer is overfilled.<br>3. An odd number of DAVFU characters has been loaded. |
| DBLCNT (LSB), DBLCTA (MSB) | DAVFU Buffer Length Counter. This counter indicates the number of characters input during the DAVFU Transfer Operation. |
| HALTPT (LSB), HALTA (MSB) | Halt Pointer. This address pointer is two locations below the top of the Input Buffer. It is used to check when the Input Buffer is nearly full. |
| HLCNT | Halt Counter. This counter indicates the number of characters (to a maximum of 2) that will be input to the Input Buffer after the HALTPT is reached. |
| HLFLAG | Halt Flag. This flag is set when the Input Buffer is within two locations of being completely full. |
| INTCH | Interim Character Received Counter. Counts the characters received while the printer is off line. |
| LLCNT | Lines Loaded Counter. This counter records the number of complete lines in the Input Buffer to be transferred to the Print Buffer. |
| LTFLAG | Line Transfer Flag. This flag is set if a line transfer from the Input Buffer to the Print Buffer is in progress. |
| MLPT | Main Loop Pointer. Used to point to the next empty location in the Input Buffer. It is incremented each time a legal character is loaded from the user. |
| OPTST | Output Port Status. This records the last byte written to OPT (Output Port). |

TABLE 2-8. DEFINITION OF FLAGS, POINTERS AND COUNTERS (Contd)

| Item | Definition |
|---|---|
| PBPT | Print Buffer Pointer. Points to the location of the Print Buffer where the next character is to be loaded. It is incremented with each character transferred from the Input Buffer. |
| PBTAS (LSB), PBTASA (MSB) | Print Buffer Pointer Temp. Store. The PBPT is stored here before the USART is interrogated. |
| PTBST | Port B Status. This records the last byte written to Port B. |
| RBFLAG | Reset Busy Flag. Flag used as a reminder to reset the BUSY signal and the BSFLAG. It is set when the buffer is no longer 3/4 full. |
| STATFG | Status On/Off Line Flag. |
| STPT | Start Transfer Pointer. Points to the first character of the next line in the Input Buffer to be transferred to the Print Buffer. It is incremented as each character is transferred. |
| TERADO | Terminator Address. This byte, together with STPT above, contains an address within the Input Buffer that points to the previous Line Terminator Code. |
| TRLNST | Transfer Line Status Word. This byte contains those bits of Port B which are set uniquely for each input data line.<br><br>Where:<br><br>Bit 7 = Expanded Code<br>Bit 6 = Condensed Code<br>Bit 4 = DAVFU/PRINT*<br>Bit 3 = DAVFU Fault<br>Bit 1 = Buffer Full |
| XOFFG | X-OFF Only Once Flag. This flag is set when the printer is not BUSY, and reset during the BUSY state before X-OFF is transmitted. It ensures that X-OFF is only transmitted once. |
| XONFG | X-ON Only Once Flag. This flag is set when the printer is BUSY, and reset during the NOT BUSY state before X-ON is transmitted. It ensures that X-ON is transmitted only once. |

### 2.4.3 DPC Centronics-Compatible Interface CCA (Option)

The DPC Centronics-Compatible Interface CCA presents the user system with an interface that is compatible with Centronics printers. As such, it accepts data in bit-parallel, character-serial form, using the DATA STROBE/ACKNOWLEDGE communications scheme. The following paragraphs describe the interface signals, interface timing, hardware, and sequential operation of the DPC Centronics-Compatible Interface.

a. Interface Signals

Table 2-9 lists and defines the signals connected between the user system and the DPC Centronics-Compatible Interface.

**TABLE 2-9. DPC CENTRONICS-COMPATIBLE INTERFACE SIGNALS**

| Signal | Definition | Pin Number | |
|---|---|---|---|
| | | PI | 50-Pin Interface Connector |
| SLCT (SELECT) | A printer-generated signal which indicates that the printer has been selected. When the SLCT signal is active:<br>(a) The ALARM light is off.<br>(b) The printer operator has pressed the ON LINE switch, or an octal (021) has been received via the data bus.<br>(c) The printer is ready to receive data. | 19 | 21 |
| SLCT RTN | | 20 | 5 |
| ACKNLG* | A printer-generated signal which acknowledges that the printer has received a data word. If the data word produces a busy condition, the acknowledge signal will not be generated until the busy condition is reset. | 15 | 23 |
| *ACKNLG RTN* | | 16 | 7 |

**TABLE 2-9. DPC CENTRONICS-COMPATIBLE INTERFACE SIGNALS (Contd)**

| Signal | Definition | Pin Number | |
|---|---|---|---|
| | | PI | 50-Pin Interface Connector |
| DATA STROBE* | A user-generated signal which defines when information on the data lines is stable and may be stored in the printer buffer. | 37 | 38 |
| DATA STROBE RTN* | | 38 | 37 |
| BUSY | A printer-generated signal indicating that the printer is unable to receive print or format data. A select code can be transmitted during a busy condition. | 17 | 22 |
| BUSY RTN | | 18 | 6 |
| INPUT PRIME* | A user-generated signal that clears the printer buffer and initializes the interface logic. The input prime signal is asynchronous to the interface logic. This signal does not affect print or paper motion cycles. | 43 | 31 |
| INPUT PRIME RTN* | | 44 | 15 |
| FAULT* | A printer-generated signal indicating that one of the following faults has occurred:<br>(a) Printer is out of paper.<br>(b) Shuttle is not moving.<br>(c) Printer is not selected. | 9 | 26 |
| FAULT RTN* | | 10 | 10 |
| OSCXT | A printer-generated signal that transmits a 100 kHz square wave to the user. | 13 | 24 |
| OSCXT RTN | | 14 | 8 |
| PE | A printer-generated signal that indicates printer is out of paper. | 11 | 25 |

## TABLE 2-9. DPC CENTRONICS-COMPATIBLE INTERFACE SIGNALS (Contd)

| Signal | Definition | Pin Number | |
|---|---|---|---|
| | | PI | 50-Pin Interface Connector |
| PE RTN | | 12 | 9 |
| PAPER INSTRUCTION (Optional) | This user-generated signal informs the printer that information on the data lines is to be treated as format data. This signal can only be used when the TCVFU or DAVFU option is installed; however, a data line can be terminated using the standard ASCII format codes (PAPER INSTRUCTION signal inactive) even though the TCVFU or DAVFU option is installed. | 41 | 30 |
| PAPER INSTRUCTION RTN | | 42 | 14 |
| DATA 1 | User Data | 21 | 19 |
| DATA 1 RTN | | 22 | 3 |
| DATA 2 | User Data | 23 | 20 |
| DATA 2 RTN | | 24 | 4 |
| DATA 3 | User Data | 25 | 1 |
| DATA 3 RTN | | 26 | 2 |
| DATA 4 | User Data | 27 | 41 |
| DATA 4 RTN | | 28 | 40 |
| DATA 5 | User Data | 29 | 34 |
| DATA 5 RTN | | 30 | 18 |
| DATA 6 | User Data | 31 | 43 |
| DATA 6 RTN | | 32 | 42 |
| DATA 7 | User Data | 33 | 36 |
| DATA 7 RTN | | 34 | 35 |
| DATA 8 | User Data | 35 | 28 |
| DATA 8 RTN | | 36 | 44 |

b. Interface Timing

Interface communication signals operate in the pulsed, rather than the handshaking mode. Once the DPC Centronics-Compatible Interface has been selected and no BUSY condition exists, it will communicate with the user as follows (see figure 2-20):

1. The user places data on the data lines and transmits a DATA STROBE* signal.

2. Sensing the DATA STROBE* signal, the DPC Centronics-Compatible Interface stores the data in the line buffer and sets a delay timer.

3. At the expiration of the delay time, the DPC Centronics-Compatible Interface returns an ACKNOWLEDGE* signal.

4. Sensing the ACKNOWLEDGE* signal, the user system can transmit another DATA STROBE signal.

If the user transmits a character that causes the Interface CCA to enter the BUSY state, (CR, DESLECT, or termination code), the interface communication sequence will be as follows (see figure 2-21):

5. The user system places a character on the data lines.

6. The user system transmits a DATA STROBE* signal.

7. Sensing the leading edge of the DATA STROBE* signal, the DPC Centronics-Compatible Interface decodes the character coded on the data lines.

8. After the character has been decoded, on the trailing edge of DATA STROBE*, the DPC Centronics-Compatible Interface enters the BUSY state.

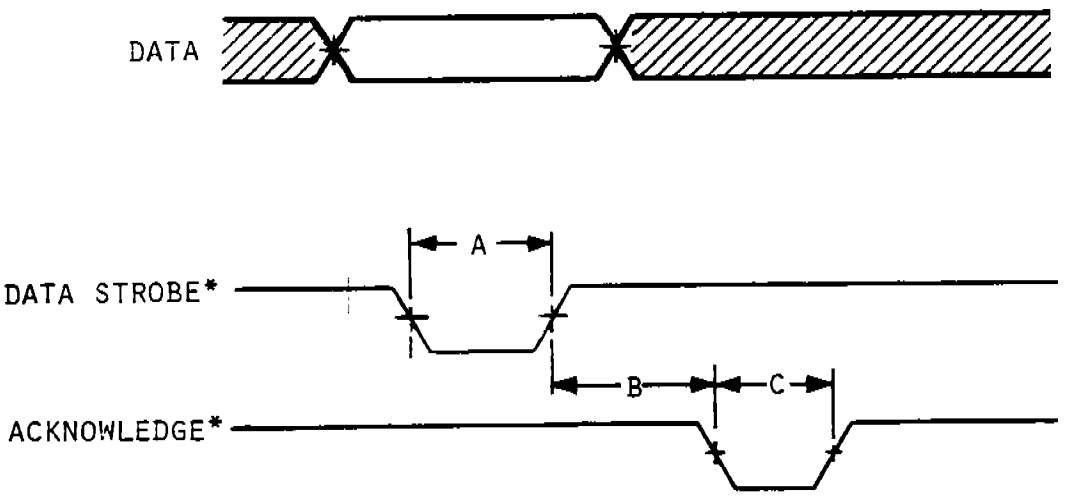
NOTE

If the character received is CR, BUSY is entered on the leading edge of DATA STROBE*.

9. After a time delay, as determined by the type of character received, the DPC Centronics-Compatible Interface terminates the BUSY state and transmits an ACKNOWLEDGE* signal to the user.

c. Interface Hardware Description (Figure 2-22)

Figure 2-22 is a simplified block diagram of the circuits that comprise the DPC Centronics-Compatible Interface. The following paragraphs describe the functions of the circuits and devices depicted.



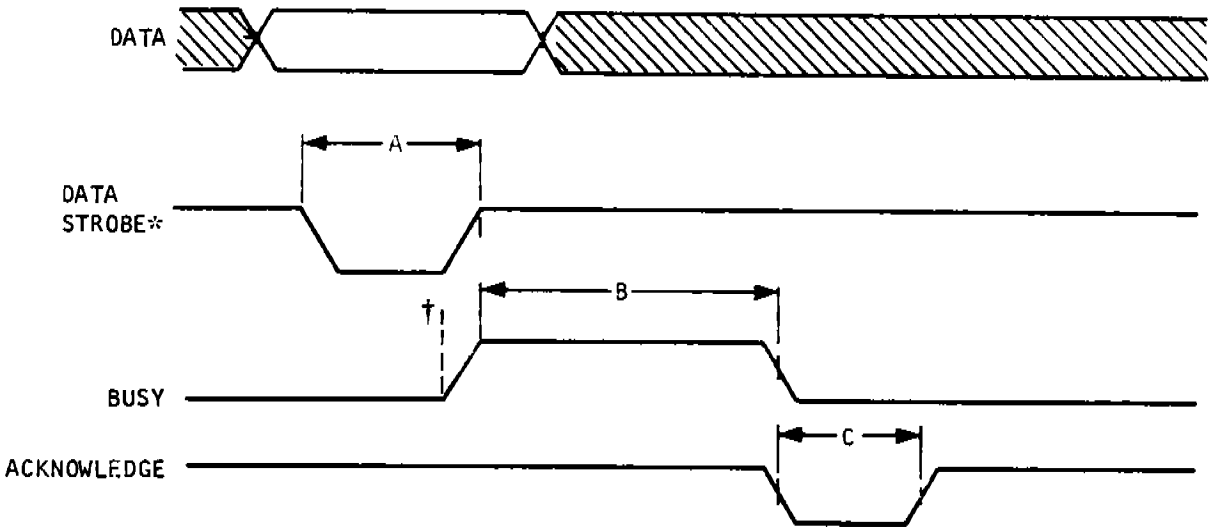

TIME B IS THE ACKNOWLEDGE DELAY

STARRED SIGNAL NAMES SIGNIFY
ACTIVE LOW SIGNAL

A = 1.0 μSEC. MAX.
= 0.5 μSEC. MIN.
B = 7 ± 1.0 μSEC.
C = 4 ± 1.0 μSEC.

= UNDEFINED AREA

Figure 2-20. Data Transfer Timing Without Busy




A = 1.0 μsec max, 0.5 μsec min
B = Duration of BUSY as defined
C = 4.0 μsec ± 1 μsec

| | RECEIVED DATA | DURATION OF BUSY |
|---|---|---|
| 1. | CR w/o Auto Line | 7.0 μsec ± 1.0 μsec |
| 2. | CR w/ Auto Line | Print & Paper Motion Cycles |
| 3. | Deselect Code | Until Printer is Selected |
| 4. | All Other Terminations | Print & Paper Motion Cycles |

STARRED SIGNAL NAMES SIGNIFY ACTIVE LOW SIGNALS
† START OF BUSY OCCURS ON TRAILING EDGE OF DATA STROBE* IN ALL CASES EXCEPT CR. WHEN RECEIVED DATA IS CR, START OF BUSY OCCURS ON LEADING EDGE OF DATA STROBE*.

= UNDEFINED AREA

245123 414

Figure 2-21. Data Transfer Timing with BUSY

1. Chip Select Decoder U48 - This device samples the five most significant bits of the Processor CCA address bus, and generates seven mutually exclusive chip select signals -- CS1 - CS4 and CS6 - CS8. The chip select signals are used to enable individual devices within the DPC Centronics-Compatible Interface. Refer to table 2-3 for the function of each chip select signal.

2. Interface Control Latch U37 - This device is connected to data bus DB1 - DB8, and forms the input half of the two-way communications path between the Processor CCA and the DPC Centronics-Compatible Interface. To latch information into U37, the Processor CCA turns on CS4, along with memory write signal MEMW. Bit designations are as follows:

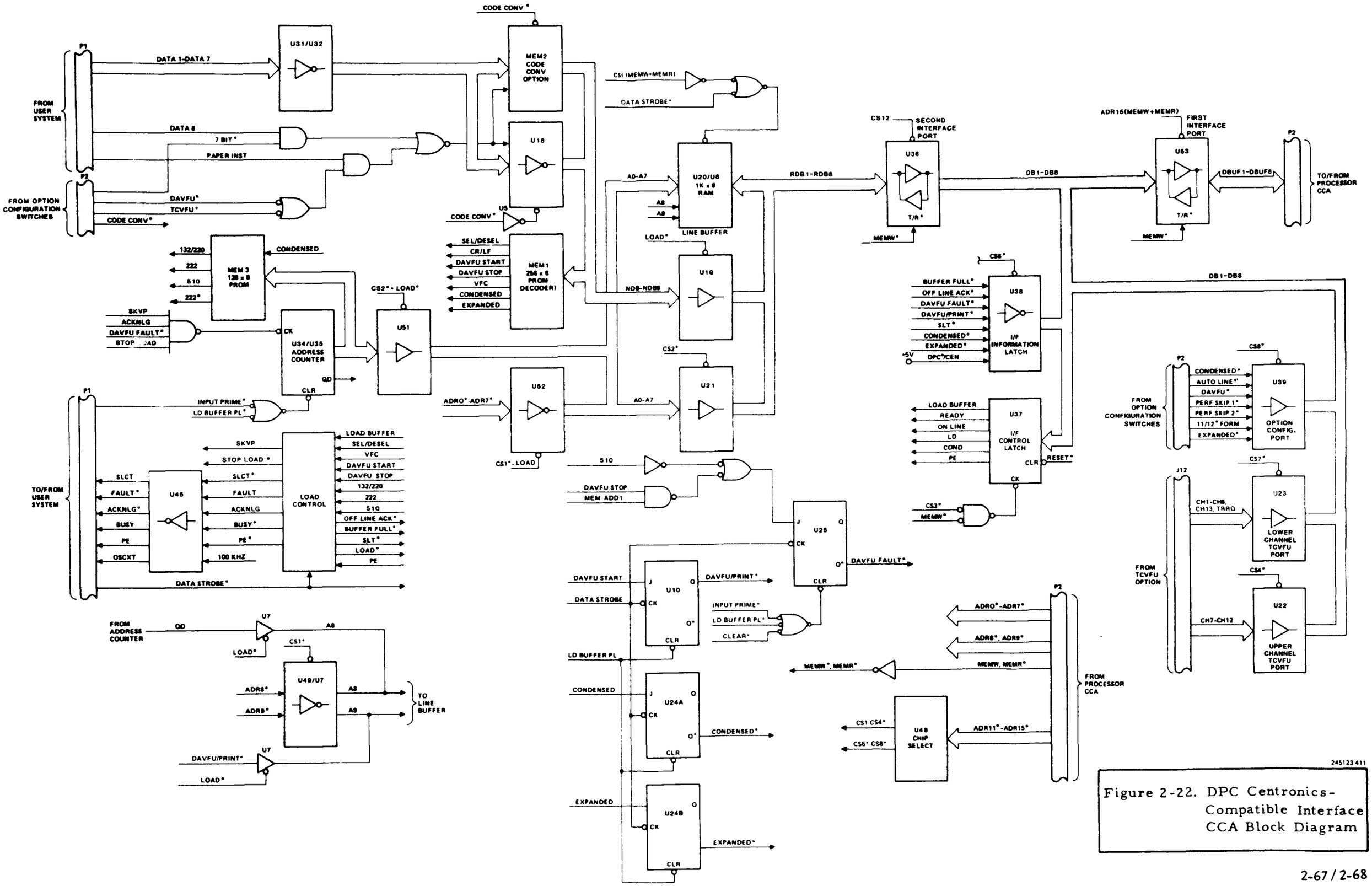
LSB DBUF1 = Load Buffer
DBUF2 = Ready
DBUF3 = On Line
DBUF4 = - -
DBUF5 = - -
DBUF6 = LD (Error)
DBUF7 = Condensed
MSB DBUF8 = PE (Paper Empty)

3. Interface Information Latch U38 - This device is connected to data bus DB1 - DB8, and forms the output half of the two-way communications path between the Processor CCA and the DPC Centronics-Compatible Interface. Since U38 has no storage capability, information is collected from different flip-flops within the DPC Centronics-Compatible Interface. To read the contents of U38, the Processor CCA turns on chip select signal CS3 along with memory read signal MEMR. Bit designations are as follows:

LSB DBUF1 = BUFFER FULL
DBUF2 = ON/OFF LINE Acknowledge
DBUF3 = DAVFU FAULT
DBUF4 = DAVFU/PRINT*
DBUF5 = SELECT
DBUF6 = CONDENSED
DBUF7 = EXPANDED
DBUF8 = DPC/CEN* (Always low in the DPC Centronics-Compatible Interface)

4. First Interface Port U53 - Connected between data buses DBUF1 - DBUF8 and DB1 - DB8, this device serves as the bi-directional data port between the Processor CCA and the DPC Centronics-Compatible Interface. The expression: ADR15 (MEMW + MEMR), implies that U53 is enabled any time the Processor CCA performs a memory write or read to or from the DPC Centronics-Compatible Interface.

5. Second Interface Port U36 - Connected between data buses DB1-DB8 and RDB1-RDB8, this device channels data bidirectionally between the line buffer U20/U8 and the Processor CCA and current address information from U21 to the Processor CCA. It is enabled by chip select signal CS12*, with MEMW*




245123 411

Figure 2-22. DPC Centronics-Compatible Interface CCA Block Diagram

controlling direction of data flow. When MEMW* is active, data flows from bus DB1-DB8 to bus RDB1-R0B8; when MEMW* is not active, data flows from bus RDB1-RDB8 to bus DB1-DB8.

6. Lower and Upper Tape Channel Ports U23 and U22 -Together, these two devices route the tape channel information from the optional TCVFU through U53 to the Processor CCA. Two memory read operations are required to transfer the full complement of TCVFU bits over the 8-bit DBUF1 -DBUF8 bus -- first, the lower half, using chip select signal CS7, followed by the upper half, using chip select signal CS4.

NOTE

The operations described in this paragraph involve the transfer of tape channel information from the TCVFU to the Processor CCA, and occur when the operator presses the tape reader switch on the TCVFU unit. Ultimately, this information is transferred from the Processor CCA to the DPC Centronics-Compatible Interface and is stored in line buffer U20-U8. Refer to paragraph 2.4.1f for TCVFU loading details.

7. Option Configuration Port U39 - This device transfers information from the option configuration switches that plug into the Mother Board and connect through P2 to the DPC Centronics-Compatible Interface. To read the contents of the option configuration switches, the Processor CCA performs a memory read operation with the address bits configured for CS8. With CS8 active, the path is open between U39 and DBUF1 - DBUF8 through U53.

8. Last Address Port U21 - This device channels the contents of the address counter U34/U35 to the Processor CCA. At the end of a data load operation, the address counter always points to the line buffer location where the last character is stored. During buffer interrogate, the Processor CCA examines each location of the line buffer, starting with the location pointed to by the address counter. To accomplish this, the Processor CCA performs a memory read operation, with the address bits configured for CS2. With CS2 active, U21 along with U51 and U36, are enabled, opening the path between the address counter and data bus DBUF1-DBUF8.

9. Buffer Driver U19 - This driver channels user data to the line buffer U20-U8. During data load operations, signal LOAD* is active, opening the path from data bus NDB1-NDB8 through U19 to DATA BUS RDB1-RDB8. Data on NDB1-NDB8 is always in ASCII form.

10. Line Buffer U20-U8 - The line buffer is a 1K x 8 RAM, used for storing print and VFU data. It is accessible, on a time-shared basis, to the circuits internal to the DPC Centronics-Compatible Interface as well as to the Processor CCA. When ASCII-coded user data is under internal control, as specified by LOAD*1, it is channelled through U19 and written into a location in the line buffer specified by address bits A0 - A9 and clocked by DATA STROBE*. In this case, the address bits are obtained in part from the address counter (U51 enabled),

and in part from flip-flop U10 (DAVFU/PRINT*), through U47. Address bit A9 is low when the data is a print or control character, selecting the lower half of buffer locations. Address bit A8 is obtained from the most significant address counter flip-flop U34.

When under control of the Processor CCA, as specified by CS1, data is either written into or out of the line buffer. Direction of data flow is controlled by mutually exclusive signals MEMW and MEMR, and the data is channeled between buses RDB1-RDB8 and DB1-DB8, through U36. With CS1 active, chip U51 is disabled and chips U52 and U49/U7 are enabled. Accordingly, buffer location address is determined by the configuration of buffer address bits ADR0-ADR9. The Processor CCA writes into the line buffer during buffer interrogate or when storing TCVFU data. Typically, data is read out of the line buffer when printing.

11. Address Counter Driver U51 - This device channels eight of the address counter bits A0-A7 to either the line buffer or to the Processor CCA. When loading user data, LOAD* is active and CS2 is inactive, and the line buffer location address is channeled from the address counter through U51 to the line buffer. During buffer interrogate, LOAD* is inactive and CS2 is active, and the address counter points to the last buffer location where the control character is stored. Accordingly, this information is channeled through U51, U21, and U36 to data bus DBUF1-DBUF8, and then to the Processor CCA.

12. ASCII Inverter U18 - This device is active when the printer operates without code conversion. It inverts ASCII-coded user data to bus NDB1 - NDB8, which is destined for the line buffer.

13. Code Converter MEM2 (Optional) - This device is active when the printer operates with code conversion. It converts user data of a specified code into ASCII format to bus NDB1 - NDB8, which is destined for the line buffer.

14. User Data Inverter U31-U32 - This device is active during data load, and is used to invert and condition user data of any code destined for either U18 or MEM1, as applicable.

15. Data Decoder MEM1 - This 256 x 8 PROM monitors user data at the NDB1 - NDB8 level for the presence of a special character. By definition, a special character is anything other than a print character, and includes the following:

(a) SEL/DESEL - The user has selected or deselected the printer.

(b) CR/LF - The user has transmitted a carriage return or a line feed.

(c) DAVFU START

(d) DAVFU STOP

(e) VFC - The user has transmitted a vertical format code accompanied by a paper instruction signal. Valid only when either TCVFU or DAVFU option is incorporated in the printer.

(f) CONDENSED - User-programmed horizontal pitch.

(g) EXPANDED - User-programmed horizontal pitch.

16. Count Decoder MEM3 - This 128 x 8 PROM monitors the output of the address counter for critical counts, as follows:

(a) 132/220 = Top Count, respectively for normal or condensed horizontal pitch.

(b) 222 = Maximum buffer load.

(c) 510 = Maximum DAVFU count.

17. Address Counter U34-U35 - Together with U25, U34-U36 forms a 9-bit binary counter with a capacity of 512. Clocked by signal ACKLG in a binary sequence, it is used during data load to form the line buffer address bits A0-A8. Bit A9 is controlled by flip-flop U10. Counter U34-U35 is turned off when signal SKVP is inactive, when signal DAVFU FAULT* is active, or when signal STOP LOAD* is active. Signal SKVP is inactive when either a condensed or expanded code is received, or when a CR code is received and auto line feed is not in effect. Signal DAVFU FAULT* is obtained from flip-flop U10. Signal STOP LOAD* is active when the total number of print characters exceed 222.

Counter U34-U35 is initialized at the start of the data load cycle by signal LD BUFFER PL*, or when the user activates signal INPUT PRIME*. When initialized, counter U39-U35 is preset to a count of 1, so that user data is never loaded in location 0 of the line buffer.

18. DAVFU/PRINT* Flip-Flop U10 - Flip-flop U10 defines the nature of the data supplied by the user during the data load cycle. When reset, it indicates that the current user data consists of print information. Reset initially by signal LD BUFFER PL*, flip-flop U10 will stay reset unless A DAVFU START code is detected by MEM2. On detection of a DAVFU START code, U10 sets and remains set for the duration of that data load cycle. Signal DAVFU/PRINT* is used during the data load cycle to form the most significant line buffer address bit A9. It is also used as a status bit channeled through U38 to the Processor CCA.

19. DAVFU FAULT* Flip-Flop U25 - This flip-flop is set when a DAVFU fault condition is detected, and is used as one of the status bits channelled through U38 to the Processor CCA. DAVFU fault condition occurs when the number of DAVFU characters supplied by the user is odd, or when the number of DAVFU characters exceeds 510.

20. Condensed, Expanded Flip-Flops U24A and U24B - These flip-flops store horizontal pitch information specified by the user in the form of horizontal pitch commands. The user may transmit either of the two horizontal pitch commands at any time during the data load cycle. From the flip-flops, the information is channelled through U38 to the Processor CCA. Then, during the subsequent print cycle, the entire line is printed with a horizontal pitch as specified. At the start of the next data load cycle, flip-flops U24A and U24B are cleared by LD BUFFER PL*.

21. Load Control - The load control is a group of circuits that controls sequential operation of the DPC Centronics-Compatible Interface. Its main function is to ensure that user-supplied print and DAVFU data is loaded in appropriate locations within the line buffer.

d. Sequential Operation (Figure 2-23)

The following paragraphs describe the sequence of major events involved in the operation of the DPC Centronics-Compatible Interface. Sequential operations are, for the most part, under control of the load control circuit group, shown in the block diagram in figure 4-22. The following topics are included, each keyed to a flow diagram:

General Operation

Data Load Cycle

User-Controlled Select/Deselect

1. General Operation (Figure 2-23) - Following initialization, the DPC Centronics-Compatible Interface is in an inactive state, monitoring the condition of the ON LINE signal. When the Processor CCA activates the ON LINE signal, an ON LINE ACKNOWLEDGE signal is returned to the Processor CCA. No further action occurs until the Processor CCA activates the LOAD BUFFER signal. Upon receipt of signal LOAD BUFFER, flip-flops LOAD and SLT are set, and BUSY reset. Then, on the trailing edge of LOAD BUFFER, flip-flop BUFFER FULL is also reset. The condition LOAD BUFFER FULL* implies that the DPC Centronics-Compatible Interface is now in the data load cycle, and the line buffer cannot be accessed by the Processor CCA. The condition SLT BUSY* informs the user that data can now be accepted.

During the data load cycle, user data is loaded, one character at a time, in the line buffer. The data load cycle ends upon receipt of a termination code (LF, CR, FF, or VFC), or when maximum count is reached and auto print is enabled. Auto print is a switch-selected feature that automatically terminates the data load cycle upon receipt of 132 characters (normal print) or 220 characters (condensed print).

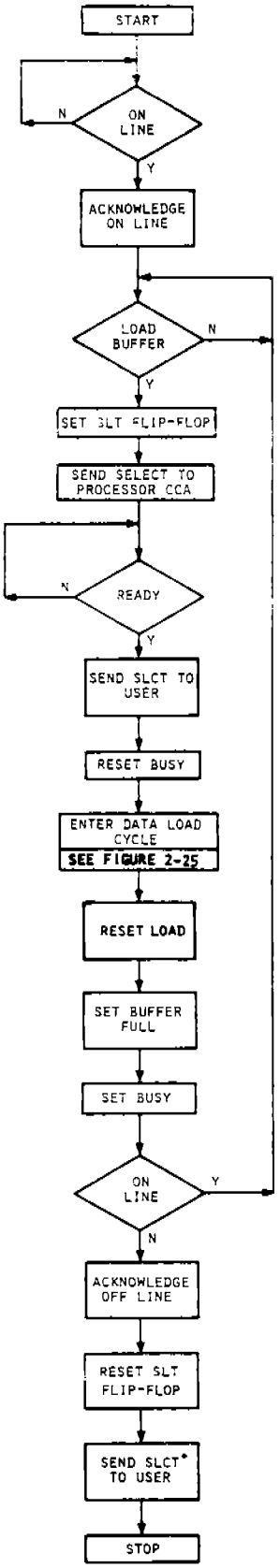



Figure 2-23. DPC Centronics-Compatible Interface CCA General Flow Diagram

NOTE

Should the Processor CCA go off line while the DPC Centronics-Compatible Interface is in the midst of loading data, the off line signal will not be acknowledged until the completion of the data load cycle.

Following completion of the data load cycle, flip-flops BUSY and BUFFER FULL are set, and LOAD is reset. The condition BUFFER FULL informs the Processor CCA that user data is now present in the line buffer and available for printing. Signal BUSY informs the user that further data will not be accepted until the BUSY condition has been lifted.

The on line signal is next monitored for a possible off line condition. If ON LINE is still high, the sequence loops back to the LOAD BUFFER decision block. If ON LINE is low, it is acknowledged immediately. Flip-flop SLT is then reset, informing the user that the printer is deselected.

2. Data Load Cycle (Figure 2-24) - The cycle begins when the user raises DATA STROBE, indicating that a character is available on the data lines. On the rising edge of DATA STROBE, an acknowledge delay timer is started, and the character is stored in location 1 of the line buffer. In addition, the character just stored in the line buffer is examined for the presence of special codes, such as a condensed or expanded code or a DAVFU start code. If applicable, a test is also made to determine if a DAVFU fault exists. If any of these conditions is encountered, the applicable flip-flop is then set on the trailing edge of DATA STROBE. Otherwise, the character is tested for CR. If CR is received but not enabled, the BUSY flip-flop is set and the BUSY timer is started. When the BUSY timer expires, the BUSY flip-flop is reset. If CR is received and enabled, if any other control character (FF, LF, or VFC) is detected, or if a maximum count is reached and AUTO TERM is enabled, the acknowledge delay timer is tested. When the acknowledge delay timer expires, the DATA STROBE is acknowledged, and the data load sequence exits and returns to the general sequence.

Under any other circumstances, such as no control character and no maximum count, the sequences do not exit but loop back toward the DATA STROBE decision box. First, the acknowledge delay timer is monitored and, when expired, the DATA STROBE is acknowledged. If no skip count condition exists, the address counter is incremented. Skip count condition exists if any of the following has been detected:

Condensed or expanded code

DAVFU error

Carriage return code (CR) was raised, but the CR function is disabled.

3. Select/Deselect (Figure 2-25) - Before the DPC Centronics-Compatible Interface can receive data from the user, it must be selected. The DPC Centronics-Compatible Interface can be selected either by the operator pressing the ON LINE switch or by the user transmitting a select code (octal 021). Once

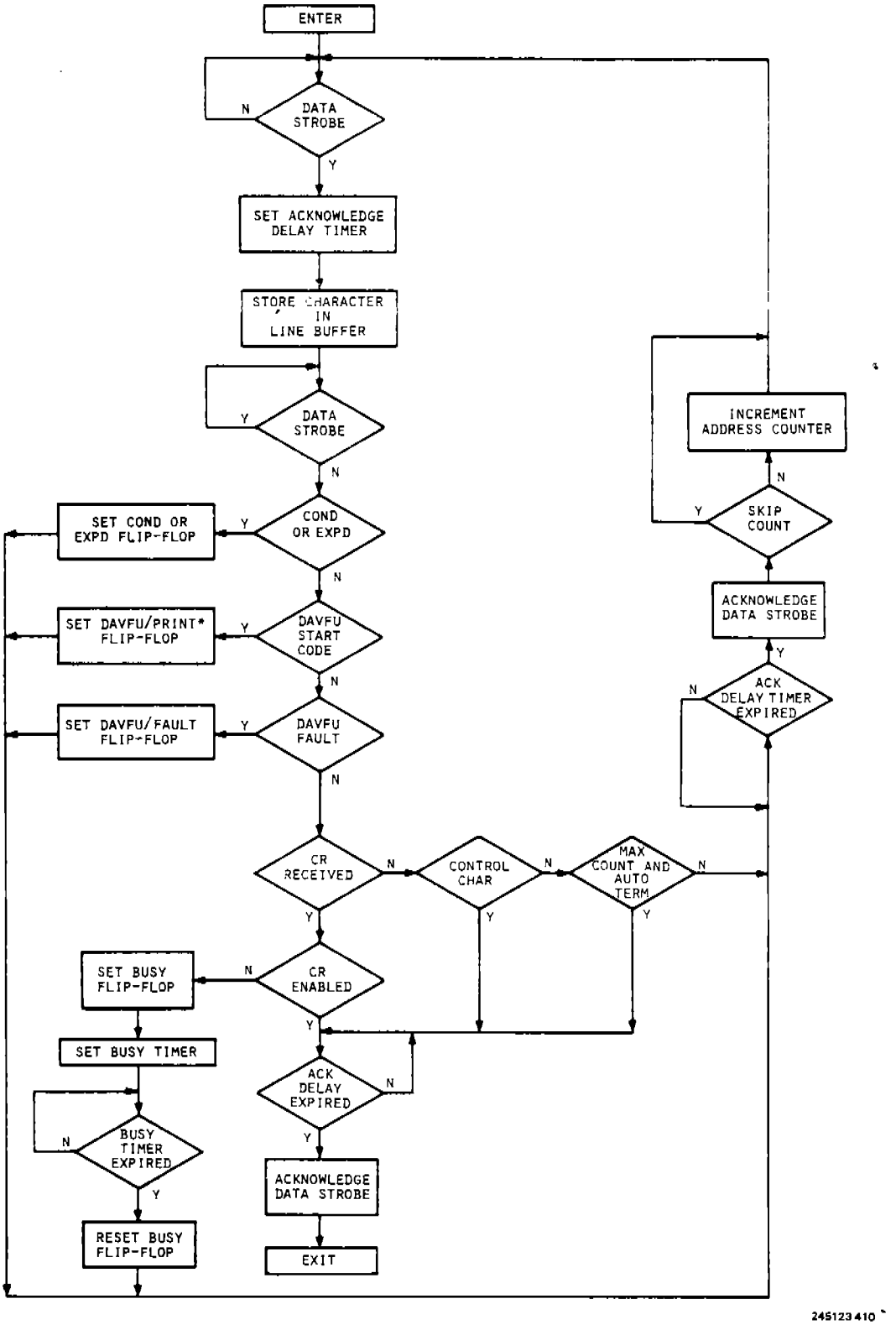



Figure 2-24. DPC Centronics-Compatible Interface Data Load Cycle

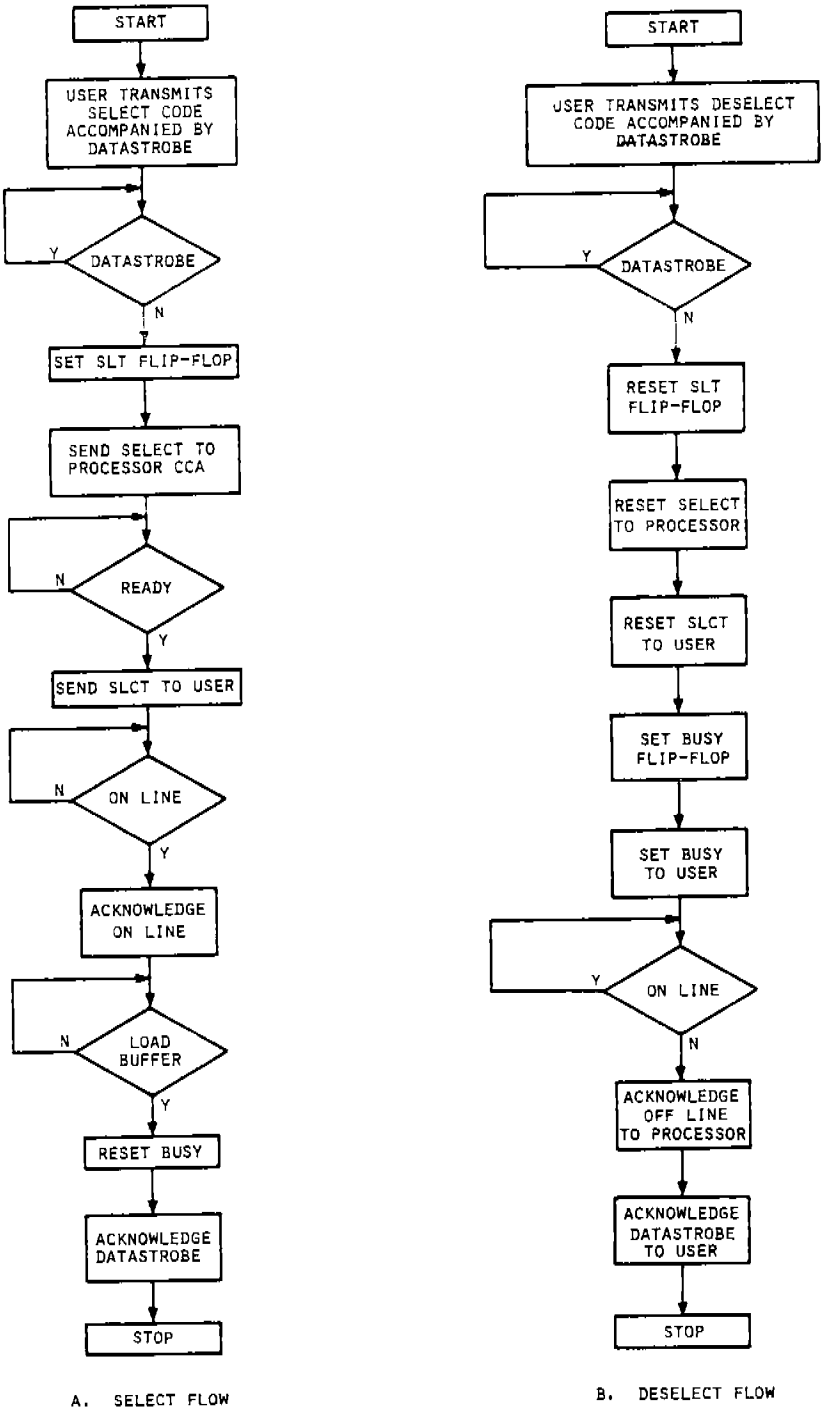



Figure 2-25. Select and Deselect Data

selected, the DPC Centronics-Compatible Interface can be deselected either by the operator pressing the ON LINE switch or by the user transmission of a deselect code (octal 023). The general flow diagram shown in figure 2-23 assumes that the select/deselect function was effected by the operator pressing the ON LINE switch. The sequence shown in figure 2-25 depicts user-transmitted select/deselect codes and is described in the following paragraphs:

(a) Select (Figure 2-25) - The sequence begins when the user transmits a select code accompanied by DATA STROBE. On the trailing edge of DATA STROBE, flip-flop SLT is set, and a SELECT signal is transmitted to the Processor CCA. Assuming that READY is active (no further action will take place if READY is inactive), signal SLCT is transmitted to the user, indicating that the DPC Centronics-Compatible Interface is selected. However, at this point, the BUSY flip-flop is still set, and data cannot be accepted from the user.

At a later point in the sequence, the Processor CCA will respond to the SELECT signal transmitted earlier by raising signal ON LINE. With ON LINE high, an acknowledge signal is returned to the Processor CCA. In response, the Processor CCA transmits a LOAD BUFFER signal. With LOAD BUFFER high, the BUSY flip-flop is reset, and the DATA STROBE signal is acknowledged, indicating that the DPC Centronics-Compatible Interface is now ready to receive data from the user.

(b) Deselect (Figure 2-25) - Action starts when the user transmits a deselected code accompanied by DATA STROBE. On the trailing edge of DATA STROBE, flip-flop SLT is reset. With SLT reset, signal SELECT is reset to the user. At the same time, flip-flop BUSY is set, and signal BUSY is transmitted to the user.

Later in the sequence, the Processor CCA responds by dropping the ON LINE signal. With ON LINE low, an OFF LINE ACKNOWLEDGE signal is returned to the Processor CCA.

NOTE

Should the user transmit a DESELECT code during a data load cycle, no OFF LINE ACKNOWLEDGE signal will be transmitted to the Processor CCA at this point.

Following acknowledgement of the OFF LINE signal, DATA STROBE is acknowledged, completing the DESELECT sequence.

## 2.5 PROCESSOR CCA (Figure 2-26)

The following paragraphs contain detailed functional descriptions of the Processor CCA. The Processor CCA is a microprocessor-based pre-programmed computer that functions as the printer's controller. As shown in the simplified block diagram in figure 2-26, the Processor CCA is interfaced with the other circuit card assemblies via the interface (I/F) port and input/output (I/O) port. The following

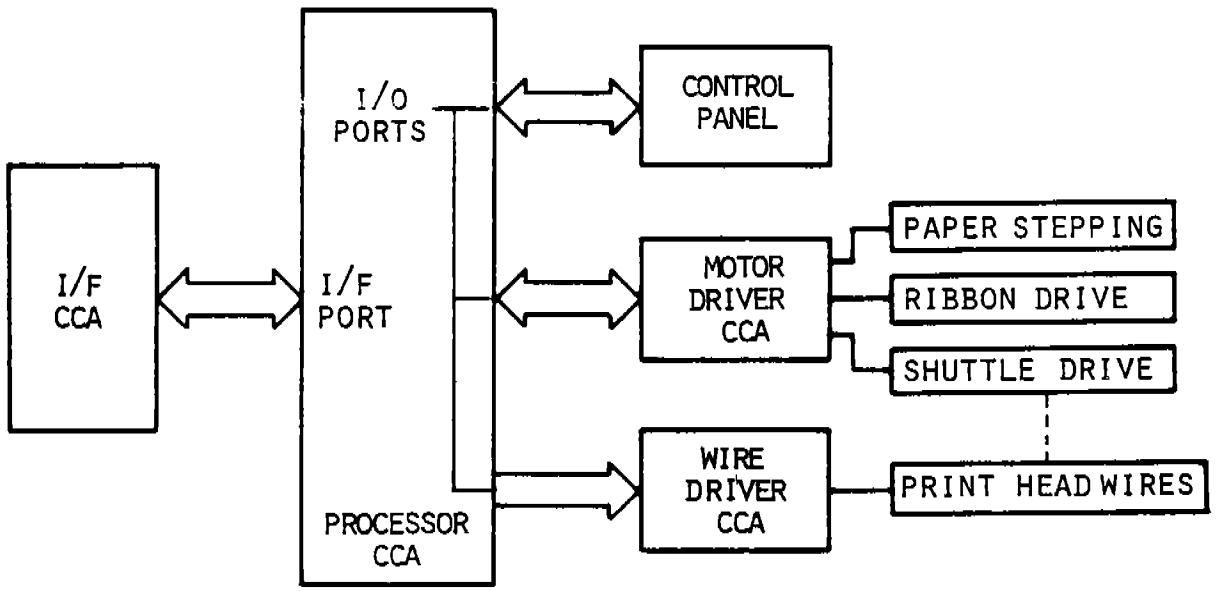



Figure 2-26. Simplified Block Diagram of Processor CCA Interface and Communication Ports

discussion of the Processor CCA's control over the I/F and I/O port communications assumes that the circuit card assemblies are integrated as a system. Detailed logic diagrams are provided in volume II of this manual.

2.5.1 Functional Organization (Figure 2-27)

The Processor CCA is organized as shown in figure 2-27 and is comprised of the following functional elements:

CPU and Control Section

Program Memory

Character Generators

I/F Port Transceiver

I/O Port Transceiver

Memory and I/O Decoding Logic

Status and Data Registers

Address and Communications Bus Structure

a. CPU and Control Section

The CPU and Control Section is comprised of the 8224 Clock Generator, the 8228 system controller, and the 8080 Control Processing Unit (CPU). These three devices synchronize and control all printer operation. Operating instructions read from program memory are carried to the 8080 microprocessor chip, via the system controller, over the internal data bus (D bus). The 8-bit data bus is connected to both I/F and I/O port transceivers, thereby establishing a communication link between the 8080 microprocessor chip and any addressable device.

The two basic operations performed by the CPU and Control Section are the read and write instructions. Information is read into the 8080 microprocessor chip, is processed, and is then written out to one of the devices on the Processor CCA I/F or I/O port. The signals MEMORY READ and MEMORY WRITE control direction of data flow.

Since the data bus is shared by most of these devices, each device must have tri-state outputs and must remain in the off state until enabled. Each device is assigned a 16-bit code address. When the 8080 microprocessor chip outputs the address of a device, that device becomes enabled, and information may be read from or written into it.

1. Control Signal Definitions - Table 2-10 contains a list of signals and their definitions used by the CP and Control Section.

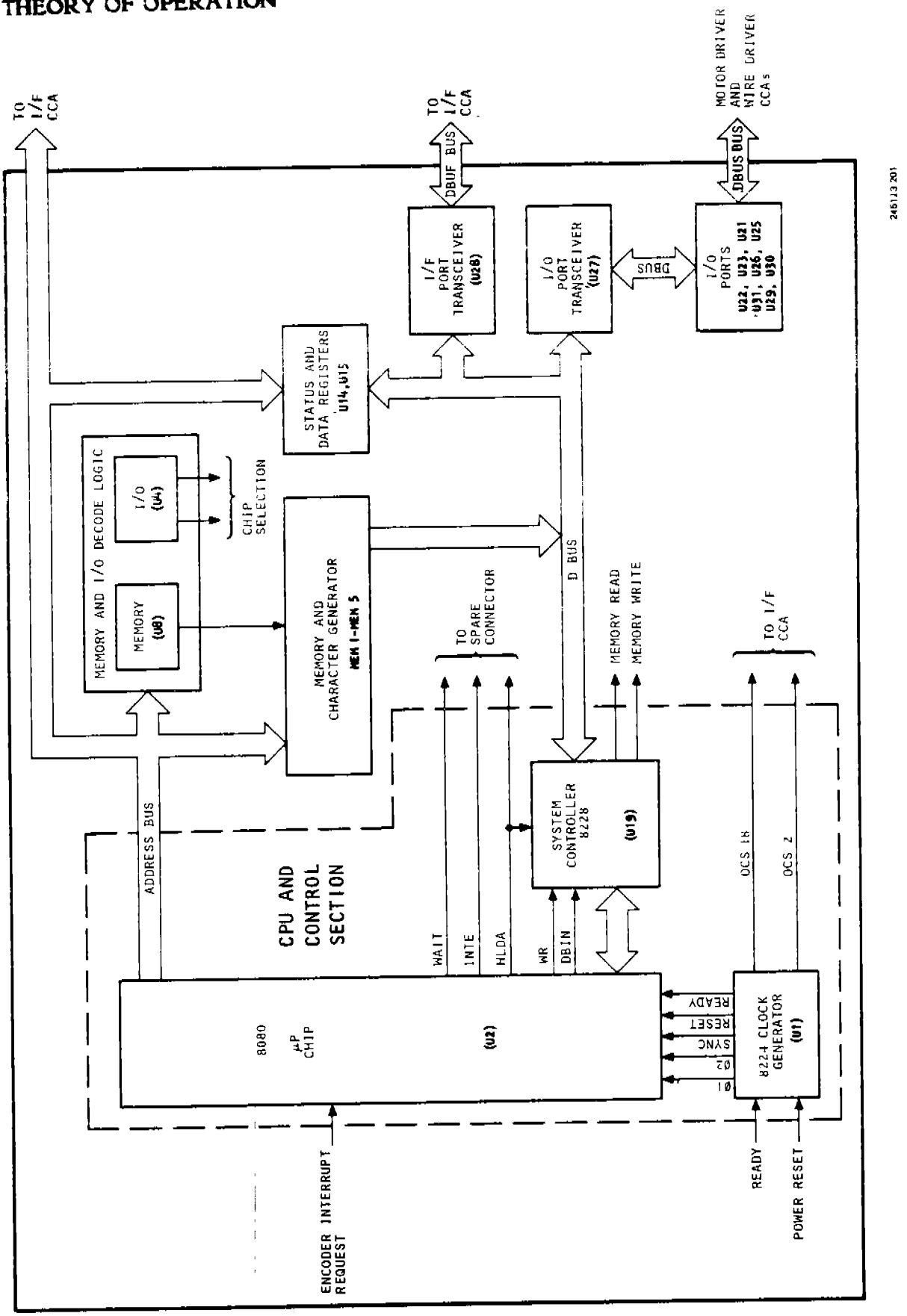



Figure 2-27. Processor CCA Functional Organization Block Diagram

TABLE 2-10. CPU AND CONTROL SECTION SIGNALS

| Signal | Definition |
|---|---|
| INT | Interrupt - counts the encoder marks. |
| INTE | Interrupt Enable - the 8080 microprocessor chip will acknowledge interrupts. |
| INTA | Interrupt Acknowledged - causes the program to jump to the proper point upon receipt of the encoder marks. |
| WAIT | A response that the 8080 microprocessor chip is in an idle mode. |
| 01 | The 2 mHz clock, 110 ns on, and 385 ns off (0-12V). |
| 02 | The 2 mHz clock, 275 ns on, and 220 ns off (0-12V). |
| RESET | A clear signal to the 8080 microprocessor chip resulting from the power up delay signal POWER RESET* to the 8224 clock generator. |
| SYNC | Output by the 8080 microprocessor chip to mark the start of the instruction cycle. |
| 02TTL | 0-5 volt Phase 2 output. |
| OSC | The 18 mHz output. |
| WR* | A write instruction is being performed. |
| DBIN | Data Bus In, a read instruction is being performed. |
| BUSEN* | The chip enable for the system controller. |
| MEMW* | Write contents of the Data Bus into a device. |
| MEMR* | Read contents of a device onto the Data Bus. |
| STATUS STROBE* | A low true construct of SYNC or POWER RESET* which allows the system controller to latch status bits and to reset automatically on power up. |

2. Operating States - This paragraph describes the 8080 microprocessor chip operating states: Write Operation, Read Operation, Interrupt Operation, Ready Condition, Reset Condition, Sync Operation, and Bus Enable.

(a) Write Operation - Signal WR* will go low whenever a write instruction is performed, allowing information from the microprocessor chip to pass through the system controller and onto the data bus.

(b) Read Operation - Signal DBIN (Data Bus In) goes high when information on the data bus is to be received by the 8080 microprocessor chip.

(c) Interrupt Operation - When enabled, the 8080 microprocessor chip can be interrupted by signal INT, which is used to count the encoder marks as the shuttle is moving. After the interrupt has been serviced, the 8080 microprocessor chip will resume normal operation at the point in the program where it was interrupted.

(d) Ready Condition - Signal RYDIN to the clock generator is synchronized and passed onto the 8080 microprocessor chip when a ready condition exists. Without the READY signal, the microprocessor chip will be in a WAIT or IDLE mode.

(e) Reset Condition - Signal POWER RESET* (Reset into the Clock Generator) is synchronized and set to the 8080 microprocessor chip as RESET, thereby clearing the microprocessor chip set and starting program execution at address zero.

(f) Sync Operation - Before each instruction is performed, the 8080 microprocessor chip conditions the control bus by outputting signal SYNC to the Clock Generator, where it is synchronized and sent as signal STATUS STROBE to the System Controller. This information is latched into a register that outputs the contents of the control bus.

(g) Bus Enable - Signal BUSEN* (Bus Enable) will enable the System Controller when low.

3. CPU and Control Section Timing - All operations performed by the 8080 microprocessor chip must be synchronized. The Clock Generator establishes the timing and synchronization for the following signals:

(a) Clock 01-02 - The Clock Generator is crystal controlled and outputs a two-phase clock to the 8080 microprocessor chip to establish the Phase 1 and Phase 2 timing.

(b) Oscillator - The oscillator output (OSC) from the Clock Generator is the frequency of the crystal, which is nine times faster than the system's rate of operation.

(c) TTL 02 - Signal TTL is the logic level Phase 2 clock.

4. 8224 Clock Generator - At the start of the print cycle, the 8080 microprocessor chip issues status information on its data bus on the type of action to take place during that cycle. By bringing the SYNC signal from the CPU and Control Section and gating it with an internal Phase 1A timing signal, a low

strobe is derived. This occurs at the start of each print cycle, as soon as the status information is stable on the bus. Signal STSTB* (Status Strobe) connects directly to the 8228 system controller.

Power up reset signal POWER RESET* also generates STSTB* which automatically resets the System Controller.

The generation of the automatic system reset and start up upon initial power up is accomplished by the 8224 Clock Generator. An external RC network is connected to the RESIN* input. The slow transition of the power supply rise is sensed by an internal Schmitt trigger. This circuit converts the slow transition into a clean, fast edge when its input reaches a predetermined value. The output of the Schmitt trigger is connected to a D-type flip-flop which is clocked by the Phase 2D internal timing signal. The flip-flop is synchronously set, and the RESET signal is withdrawn from the 8080 microprocessor chip. The RYDIN* (Ready In) signal is connected to a D-type flip-flop and is also clocked by Phase 2D. Its output, READY, is sent to the 8080 microprocessor chip. The 8224 single chip Clock Generator/Driver contains the following:

(a) Crystal-Controlled Oscillator - Two inputs are provided for the crystal connections XTAL1 and XTAL2. The selection of the external crystal frequency depends mainly on the speed at which the 8080 microprocessor chip is to be run. Basically, the oscillator operates at nine times the desired microprocessor chip speed. The crystal selected for the printer is 18 mHz.

(b) Clock Generator - The Clock Generator consists of a synchronous divide-by-nine counter and all the associated decode gating needed to create the waveforms of the two 8080 microprocessor chip clocks and auxiliary timing signals. The waveform generated by the decode gating is a 2-5-2 digital pattern.

The Phase 1 and Phase 2 clocks generated can be thought of as consisting of units based on the oscillator's frequency. Assume that one unit equals the period of the oscillator frequency. By multiplying the number of units contained in a pulse width or delay, times the period of the oscillator frequency, the approximate time in nanoseconds can be obtained.

(c) High Level Drivers - The outputs of the Clock Generator are connected to two high level drivers for direct interface to the 8080 microprocessor chip. TTL level Phase 2 is also generated for external timing purposes.

(d) Auxiliary Logic Functions - Several other signals are generated internally so that timing of the auxiliary flip-flops (READY, RESET, and STATUS STROBE) can be achieved.

5. 8228 System Controller - The 8228 is a single chip system controller and data bus for the microprocessor. It generates all control signals required to interface directly with RAM, ROM, and devices on both I/F and I/O ports. The bi-directional bus driver is controlled by signals from the gating array so that proper bus flow is maintained, and its outputs can be forced into their high impedance state (tri-state) for direct memory accessing activities.

At the start of each print cycle, the 8080 microprocessor chip issues on its data bus status information that indicates the type of activity that will occur during the cycle. The system controller stores this information in a status latch when the STSTB* (status strobe) information goes low. The output of the status latch is connected to the gating array and is part of the control signal generation.

(a) Gating Array - The gating array of the 8228 system controller generates control signals MEMR*, MEMW*, I/O R*, I/O W*, and INTA* by gating the outputs of the status latch with signals DBIN*, WR*, and HLDA*, from the 8080 microprocessor chip.

(b) Read Operation - The read control signals MEMR*, I/O R*, and INTA* are derived from the logical combination of the appropriate status bits and the DBIN input from the 8080 microprocessor chip.

(c) Write Operation - The write control signals MEMW* and I/O W* are derived from the logical combination of the appropriate status bits and the WR* input from the 8080 microprocessor chip.

(d) Interrupt - The ENC INT REQ* interrupt signal is automatically gated onto a bus internal to the 8080 microprocessor chip. Each interrupt will cause a jump to a specified location in the program memory. The system controller is set up so that when DBIN input is active, the instruction is gated onto the internal data bus (D Bus) when ENC INT REQ* is acknowledged.

(e) Bus Enable - The BUSEN* (bus enable) input will enable the system controller when low. Since a single system controller is used on the printer, this signal is tied to ground.

b. Program Memory

The program memory and character generator consists of Programmed Read Only Memory chips (PROMs) MEM1 through MEM5. A map of this memory structure is shown in figure 2-28. Enabling any of the various memory devices is a function of the memory and I/O decode logic shown in table 2-12.

As shown in figure 2-28, the program memory is partitioned into dedicated segments comprising the program control section, input/output ports, status and data buffer registers, and right and left character generation segments.

1. Program Control Section - The program control section is the main portion of the memory, coordinating the sequence of operation for correct printer operation. The program control section performs the following tasks:

Monitors all printer switches.

Controls two-way status and data exchange with the Interface CCA.

Controls the shuttle servo motor for speed and direction.

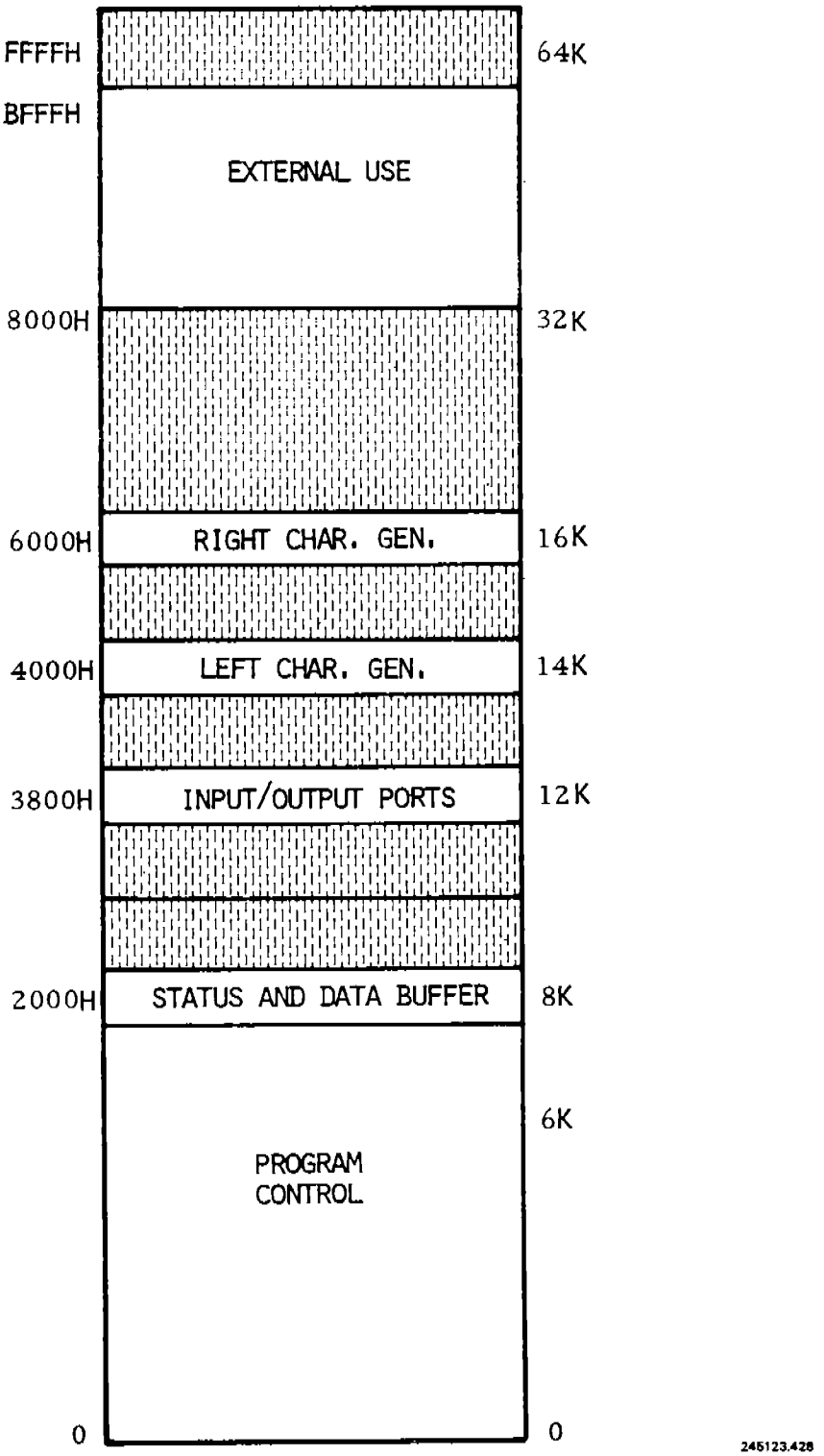



Figure 2-28. Program Memory Map

Moves paper as required by controlling the paper feed stepping motor.

Prints data by controlling the firing of the print wires.

c. Character Generators

This section of the memory contains the tables which specify the print wire(s) to be fired for each printable character. Figure 2-29 shows an example of character generation. The vertical columns (dot columns) represent seven of ten equally spaced segments of a character column. Columns eight to ten are used by the control program for character spacing. The dot column data corresponds to the encoder-generated interrupts input into the 8080 microprocessor chip. Each horizontal column represents one of seven print wires in the print head to be fired when printing a character.

Each dot column represents one byte (8 bits) of data which determines if a dot is to be printed. Since there are only seven wires per wire bank, bit 8 is always a zero. As shown in figure 2-29, dot column zero has a dot in positions 1 and 7, which corresponds to a hex 41. In dot column 6, positions 2, 3, 5, and 6 have dots which correspond to a hex 36.

The data is stored in consecutive bytes within the character generator. These are addressed by a combination of the binary equivalent of the dot column number plus the binary equivalent of the seven-bit ASCII code for the character being printed. The most significant bit of the address is a zero for the left bank and a one for the right bank. Table 2-11 provides an example of the ASCII code dot column number addressing.

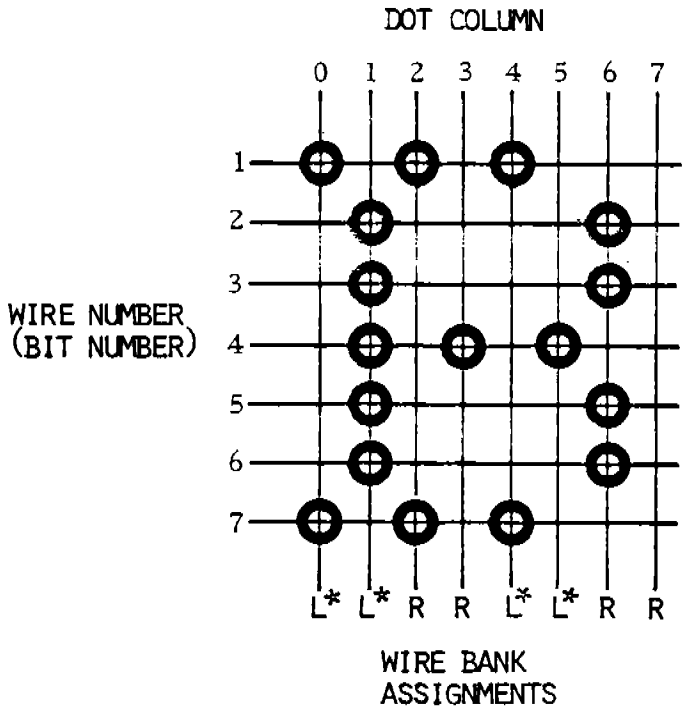
NOTE

In the M120 printer, data for each character is accessed the same way as in the M200 printer; i.e., from both the right and left halves of the character generator. However, the collected data is then printed by the same (the only) bank of print wires.

**TABLE 2-11. ASCII CODE/DOT COLUMN NUMBER ADDRESSING**

| ASCII Code | Dot Column Number | Address (Hex) | |
|---|---|---|---|
| | | Left | Right |
| 1 0 0 0 0 1 0 | 0 0 0 | 210 | 610 |
| 1 0 0 0 0 1 0 | 0 0 1 | 211 | 611 |
| 1 0 0 0 0 1 0 | 0 1 0 | 212 | 612 |
| 1 0 0 0 0 1 0 | 0 1 1 | 213 | 613 |
| 1 0 0 0 0 1 0 | 1 0 0 | 214 | 614 |
| 1 0 0 0 0 1 0 | 1 0 1 | 215 | 615 |
| 1 0 0 0 0 1 0 | 1 1 0 | 216 | 616 |
| 1 0 0 0 0 1 0 | 1 1 1 | 217 | 617 |

Note: For international characters $80_H$ - $9F_H$, bit 8 is dropped, and addressing starts at $0_H$.




| | L | R |
|---|---|---|
| 0 | $41_H$ | 00 |
| 1 | $3E_H$ | $0_H$ |
| 2 | $0_H$ | $41_H$ |
| 3 | $0_H$ | $08_H$ |
| 4 | $41_H$ | $00_H$ |
| 5 | $08_H$ | $0_H$ |
| 6 | $0_H$ | $36_H$ |

A DOT = 1
NO DOT = 0

* M200 ONLY. THE M120 HAS ONLY ONE WIRE BANK.

245123.430

Figure 2-29. Example Of Character Generator Structure

The address bus to the character generator has been arranged so that a 16-bit address will access the data for each dot column. The lower byte of the address is the same as the ASCII code for the character being printed. The lower 3 bits of the upper byte are the dot columns being printed at that particular moment. The upper byte is either a $4_H$ or a $6_H$, depending on whether the data is for the left or right bank of wires.

For dots printed by the same wire, there are a minimum of three dot columns between the dots. This spacing allows for the cycle time needed for the wires. Cycle time is the total amount of time required for a wire to go from a rest position to a full extension and then back to a rest position.

d. Interface Port Transceiver

The Processor CCA communicates with the various interface configurations described in paragraph 2.3 via the I/O port transceiver U28, using address bit A15. Control and status information and data exchanged between the Processor CCA and the Interface CCA are transferred over the 8-bit DBUF bus. The information exchanged between the two CCAs and the input/output devices which interface the Interface port transceiver is described in paragraph 2.5.3 and illustrated in figure 2-28. Another function of the Interface port transceiver is to supply status information to the optional status display using chip select signal CS16*. The interface port transceiver operation is shown in the following truth table.

| MEMR* | A15* | CS16* | Function |
|---|---|---|---|
| 1 | 0 | 1 | Write Data to I/O Port |
| 1 | 1 | 0 | Write Data to Display |
| 0 | 0 | 1 | Read Data from I/F Port |

* = Active in the low state
X = Don't care condition

e. I/O Port Transceiver (U27)

The Processor CCA communicates with the print, paper advance, ribbon advance, and shuttle movement control electronics via the I/O bus transceiver U27. A detailed description of the I/O port functions is provided in paragraph 2.5.4 and illustrated in figures 2-32 and 2-33. The I/O port transceiver is shown in the following truth table.

| CS6* | MEMR* | Function |
|---|---|---|
| 0 | 0 | Read from I/O Port |
| 0 | 1 | Write to I/O Port |

* = Active in the low state
X = Don't care condition

f. Memory and I/O Decoding Logic

A unique device within the program memory and character generator section is enabled by memory decoder U8. The memory decoder uses a 5-bit address scheme (bits 11-15) to select one of eight memory devices. I/O decoding is performed by U4, which uses a 9-bit address scheme (bits 0-3 and 11-15). Table 2-12 below lists the memory device enable signals and their functions. Refer to table 2-15 for the device enable selection signals and their functions.

TABLE 2-12. MEMORY DEVICE ENABLE SIGNALS

| Address Bit Configuration | | | | | Chip Select Signal | Function |
|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | | |
| 0 | 0 | 0 | 0 | 0 | CS1* | With CS2*, enables MEM1 |
| 0 | 0 | 0 | 0 | 0 | CS2* | With CS1, enables MEM1; enables MEM2 |
| 0 | 0 | 0 | 1 | 0 | CS3* | Enables MEM3 |
| 0 | 0 | 0 | 1 | 1 | CS4* | Enables MEM4 and MEM3 |
| 0 | 0 | 1 | 0 | 0 | CS5* | Enables U15 and U14 |
| 0 | 0 | 1 | 1 | 0 | CS6* | Enables U27 |

g. Status and Data Registers

The Status and Data Registers are random access memory chips U14 and U15. These elements are linked to form 8-bit-wide registers, used to store the status of each device that controls the printer operation and to provide temporary storage for print or VFU data. Table 2-13 lists the locations addressed by the CPU and Control Section and the function of each location.

TABLE 2-13. STATUS AND DATA REGISTER ADDRESS AND USAGE

| Address (Hex) | Usage |
|---|---|
| 2000-2085 | Processor CCA RAM used to store the self test pattern. |
| 208F | Counts the number of times used to store the self test pattern. |
| 2090 | Dot column counter. Its value is incremented (or decremented) by each encoder mark, depending on the direction in which the Motor Driver CCA is moving. |
| 2091 | Character column counter. Its value is incremented (or decremented) each time a new character is accessed. |
| 2092 | True condition bit used to determine if a switch change is real or caused by noise. |

## TABLE 2-13. STATUS AND DATA REGISTER ADDRESS AND USAGE (Contd)

| Address (Hex) | Usage |
|---|---|
| 2093 | Interface CCA RAM status register. Is set if Interface CCA is installed. |
| 2094 | Register containing the line termination code received from the Interface CCA. |
| 2095 | Shuttle Speed compressed print flag. |
| 2096 | Out of Paper Status Register. |
| 2097 | Non-underline printable character flag which is set each time a printable character is decoded. |
| 2098 | Printable character bit which is set whenever a line of data contains printable characters. |
| 2099 | No paper motion status register. Set to $01_H$ each time paper has been moved, which inhibits paper motion. |
| 209A | Expanded print bit which is set when a line of data contains an expanded code. |
| 209B | Multiple line feed bit which is set whenever a form feed or VFU command is received. |
| 209C | Underline bit which is set whenever an underline code is received. |
| 20AC | Contains print data for the right bank of wires. |
| 20AD | Contains control information for the Interface CCA (on line, load buffer, etc.). |
| 20AE | Contains print data for the left bank of wires.* |
| 20AF | Contains the ASCII code for the right bank of wires. |
| 20B0 | Contains the ASCII code for the left bank of wires.* |

*In the M120 Printer, all data are printed by the right bank of wires.

TABLE 2-13. STATUS AND DATA REGISTER ADDRESS AND USAGE (Contd)

| Address (Hex) | Usage |
|---|---|
| 20B1 | Register that contains information to determine which way to move the shuttle in order to print the next line. |
| 20B3 | Contains forms length select switch setting. Used to initialize register $20A4_H$ and update any FLS changes. |
| 20B5 | Horizontal velocity bit used to detect a change in shuttle speed. |
| 20B6 | Temporary storage register for print data. Used for expanded print. |
| 20B9 | Register that contains information calculated for seeking horizontal position of the shuttle. Used to determine the fastest way to move the shuttle to print the next line. |
| 20BB | Contains the start of line character column count value. |
| 20BC | Contains the end of line character column count value. |
| 20BD | Contains information for output port $3008_H$. |
| 20BE | Contains information for output port $3007_H$. |
| 20C0 | Counter used to detect the absence of encoder marks. |
| 20C1 | Counter used for 240 line shutoff for self test. |
| 209C | Underline bit which is set whenever an underline code is received. |
| 209D | Partial paper feed bits one and two. Set for underlining. |
| 209F | Self test bit which is set when the printer is in the self test mode. |
| 20A0 | Character column counter right. Counts multiples of 10 encoder marks for the right bank of wires. |

*In the M120 Printer, all data are printed by the right bank of wires.

TABLE 2-13. STATUS AND DATA REGISTER ADDRESS AND USAGE (Contd)

| Address (Hex) | Usage |
|---|---|
| 20A1 | Character column counter left. Counts multiples of 10 encoder marks for the left bank of wires.* |
| 20A2 | Contains the character column counter value of the first character in the line. |
| 20A3 | Contains the character column counter value of the last character in the line. |
| 20A4 | Contains the number of printable lines remaining in the form. It is decremented each time paper is moved. |
| 20A5 | Contains the number of printable lines in a form. Based on vertical pitch, forms length select switch setting, and variable format information. |
| 20A6 | Overprint counter, set to 12 initially. Decremented whenever an overprint occurs. |
| 20A7 | Contains either a carriage return, line feed, or form feed code. |
| 20A8 | Contains the number of lines for perforation skip. |
| 20A9 | Contains the upper 8 bits of print buffer address. |
| 20C2 | Register used as a timer for various printer operations. |
| 20C3 | Register used as a timer for various printer operations. |
| 20C4 | Counter used to allow only five successive reads of a vertical format tape. |
| 20C5 | Vertical format-loaded status register. Set whenever vertical format data has been loaded, or any vertical format faults have been cleared. |
| 20C6 | Contains lower byte of vertical format memory address. |

*In the M120 Printer, all data are printed by the right bank of wires.

TABLE 2-13. STATUS AND DATA REGISTER ADDRESS AND USAGE (Contd)

| Address (Hex) | Usage |
|---|---|
| 20C7 | Contains upper byte of vertical format memory address. |
| 20C8 | Lower byte of direct access vertical format counter. |
| 20CA | Forms length count value for bottom of form position. |
| 20CB | Forms length count value for top of form position. |
| 20CC | Bottom of form for perforation skip. |
| 20CD | Go to top of form for perforation skip. |
| 20CE | On line flip-flop status register. Used to check for changes in the state of the on line flip-flop. |
| 20CF | Bit set when a carriage return code terminates a line of data containing an underline code. Inhibits paper motion. |
| 20D0 | Print head shuttle position seeking bit, set whenever the shuttle is moving the print head. |
| 20D1 | Top count code used with the DPC Centronics-Compatible Interface CCA. Used with auto print feature. |
| 20D2 | Jog timer bit which is set after a jog. When set, will cause a time delay to allow the shuttle speed to settle before further movement occurs. |
| 20D3 | Double termination code bit which is set when a line of data contains a termination code only (LF, CR, or FF). |
| 20D4 | Carriage return only bit which is set when a carriage return code terminates a line of data. |
| 20D5 | CR Only flag. Set when a carriage return terminates a line of data. |
| 20D6 | CRLF flag. |

h. Address and Communications Bus Structure

The Processor CCA uses a four-bus system to address and communicate with its various internal elements, the Interface CCA, the Wire Driver and Motor Driver CCAs, and the operator control panel. The following buses comprise the address and communications bus structure: D Bus, DBUS Bus, DBUF Bus, and Address Bus.

1. D Bus - The D bus is an 8-bit bus which interfaces the CPU and Control Section with the I/O port transceiver (U27), I/F port transceiver U28, the program memory and character generator, and the status and data registers U14 and U15.

2. DBUS Bus - The DBUS Bus is an 8-bit bus which interfaces the I/O port transceiver U27 with the various I/O port devices.

3. DBUF Bus - The DBUF Bus is an 8-bit bus which interfaces the Processor CCA with the Interface CCA and the optional status display on the control panel.

4. Address Bus - The address bus is a 16-bit high true bus used for memory addressing and chip selection. The high true state is used for addressing the interior elements of the Processor CCA (bit 15 is always low). The address bus is routed through inverters and transferred to the Interface CCA in the true state. (Bit 15 must be in the high state when an internal element of the Interface CCA is to be addressed).

2.5.2 Initialization for Interface and Input/Output Port Communication

Before the I/F and I/O ports can be enabled for data transfer, wire firing, ribbon advance, and paper advance operations, the printer must be powered up and the initialization and operating status verification sequences must be performed.

a. Power Up PWR RESET*

When PWR RESET* goes active, the CPU and Control Section will perform the following functions:

1. Disable Interface Control Latch $9000_H$ by writing a $00_H$. Status is written into Status and Data Register $20AD_H$.

2. Read Option Configuration Switch data from interface port $B800_H$.

3. Write a $B3_H$ to I/O port $3008_H$ to drive the Paper Feed Stepping Motor to Phase One, and then a BE to lock the motor to Phase One. This phase of this operation is stored in Status and Data Register 3006H.

4. Read Perforation skip data from the Interface options configuration latch $B800_H$, compute the value, and store in Status and Data Register $20A8_H$.

5. If the FLSS option is installed, the value is read from I/O port 300B and stored in Status and Data Register $20B3_H$. The value is converted into the number of printable lines and stored in Status and Data Registers $20A4_H$ and $20A5_H$.

6. If the printer is of a standard configuration, the value is read from Interface Option switches $B800_H$, is computed, and stored in Status and Data Registers $20A2_H$ and $20A5_H$.

7. DBUF4 is set to Interface Control latch $9000_H$, and the status is stored in Status and Data Register $20AD_H$.

8. Outputs from I/O Port $3007_H$ are set to the high state. Signal RESET* in the high state clears the internal logic and logic on the Interface CCA.

9. The following Status and Data Registers are set as indicated: $2005_H$ = 00, $20CC_H$ = 00, $20CD_H$ = 00, and $2096_H$ = 01.

b. Initialization

The Initialization sequence is entered as a result of completing the power-up sequence, or as a result of an alarm clear condition. The sequence is as follows:

1. DBUF1 - DBFU3 are set low to Interface Control Latch $9000_H$, resetting signals ON LINE, READY, and LOAD BUFFER. The status of this operation is stored in Status and Data Register $20AD_H$.

2. DBUS is set to $32_H$ and transferred to output port $3007_H$. This operation resets flip-flops U12 and U11 on the Processor CCA and resets logic on the Interface CCA.

3. Signal CLRFF (bit 5) of input port $3009_H$ is tested for its logic state. If low, then all outputs of port $3008_H$ are set high to disable all motor operations. If high, then the following Status and Data Registers are set as indicated below:

| Register | Value |
|---|---|
| 2099 | 01 |
| 209B | 00 |
| 209C | 00 |
| 209D | 00 |
| 209F | 00 |
| 20A6 | 12 |
| 20CB | 00 |
| 20CF | 00 |
| 20D0 | 00 |

4. Signal 10/16* PITCH (bit 6) of input port $300B_H$ is tested for its logic state. If low (16 pitch) then $20_H$ is written into Status and Data Register $2095_H$ and $20B5_H$. If high (10 pitch), then $00_H$ is written into the registers.

5. Signal BAIL OPEN (bit 4) of input port $300A_H$ is tested for its logic state. If low, then the state of signal CLEAR FLOP output from U12 is tested at Input port $3009_H$. BAIL OPEN in the high state will cause the CPU and Control Section to recycle through the initialization sequence until BAIL OPEN is reset. BAIL OPEN in the high state will cause ALARM IND* of output port $3007_H$ to be enabled, and READY to be reset to Interface Control Latch $9000_H$. The new interface status word is written into Status and Data Register $20AD_H$. This cycle will continue until CLRFF of input port $3009_H$ switches to the high state. BAIL OPEN in the low state will cause GO/STOP of output port $3008_H$ to be enabled, which will initiate shuttle movement to the shuttle park position.

6. DBUF Bus is set to zero and output to the VFU/Print data line buffer $8000_H$ on the Interface CCA. The CPU and Control Section will then perform a read operation to detect any change in the status of DBUF Bus. If a change is detected, indicating the absence of any Interface CCA, Status and Data Register $2093_H$ is cleared, and output port $3008_H$ is disabled to halt any motor operation. If the DBUF Bus remains low, indicating the presence of an Interface CCA, then $01_H$ is written into Status and Data Register $2093_H$ and DBUF bit 2 (READY) is set high to Interface Control Latch $9000_H$.

c. Operating Status Verification (Figure 2-30)

After completing the Power-up and Initialization sequences, the CPU and Control Section enters into the operating status verification sequence. This sequence is re-entered each time the shuttle is parked because of a slow interface data transmission rate, a paper advance command which requires multiple line feed operations, a command which requires a change in the shuttle travel velocity, the absence of a character generator, or because of the completion of a self test operation. Completion of this sequence allows the CPU and Control Section to enable the ports for either on line or off line operation.

During this sequence, the Status and Data Registers are updated to reflect the current operating status of the I/F and I/O ports. Upon completion of this sequence, the ON LINE, READY, and LOAD BUFFER CONTROL outputs are enabled to I/F Port $9000_H$.

2.5.3 Interface Port Communication and Control (Figure 2-31)

Communication between the Processor CCA and the Interface CCA takes place over the DBUF bus. Each of the interface types described in paragraph 2.4 contains devices which are addressable by the CPU and Control Section.

As shown in figure 3-31, a given device is enabled for input or output when selected by the CPU and Control Section. Device selection is effected by the CPU and Control Section of the Processor CCA through address bus AD00-AD15. Each Interface CCA converts address bits A11-A13 into a unique chip select pulse (CS1* - CS9*) as listed in table 2-14. Address bit A15 (bit 14 is 0) must be true when any interface port chip select pulse is generated.

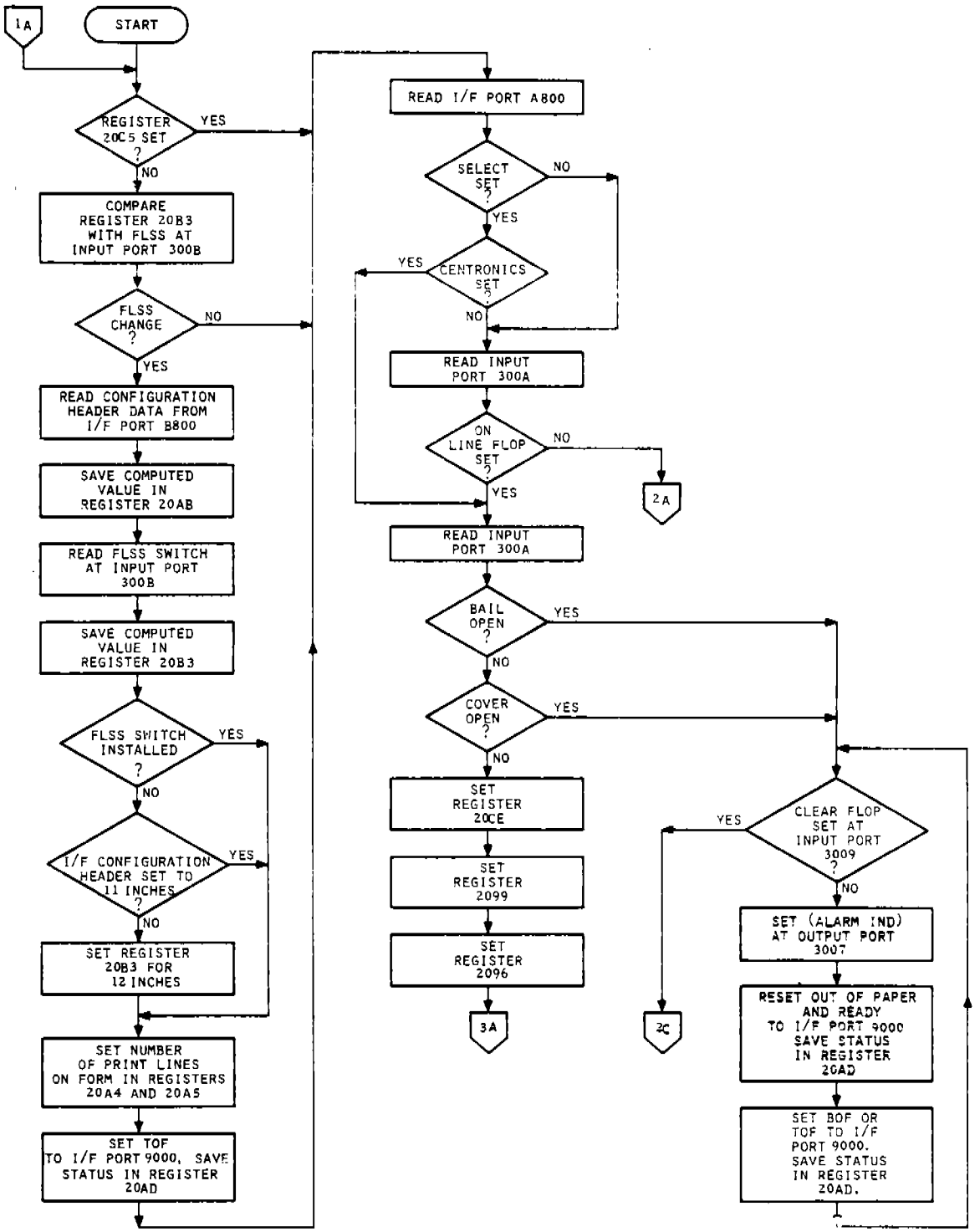



Figure 2-30A. Operating Status Verification Flow Diagram

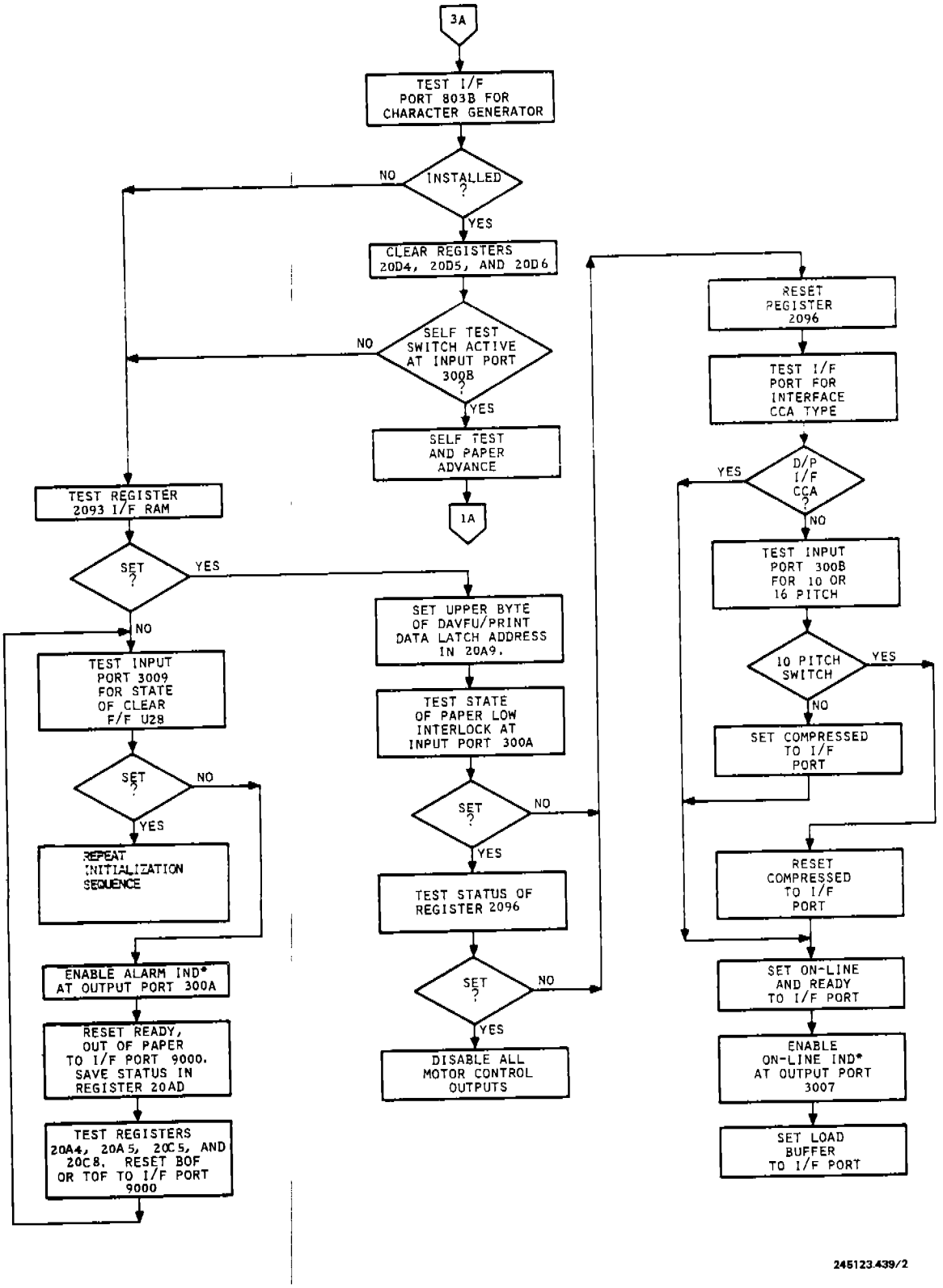



Figure 2-30B. Operating Status Verification Flow Diagram

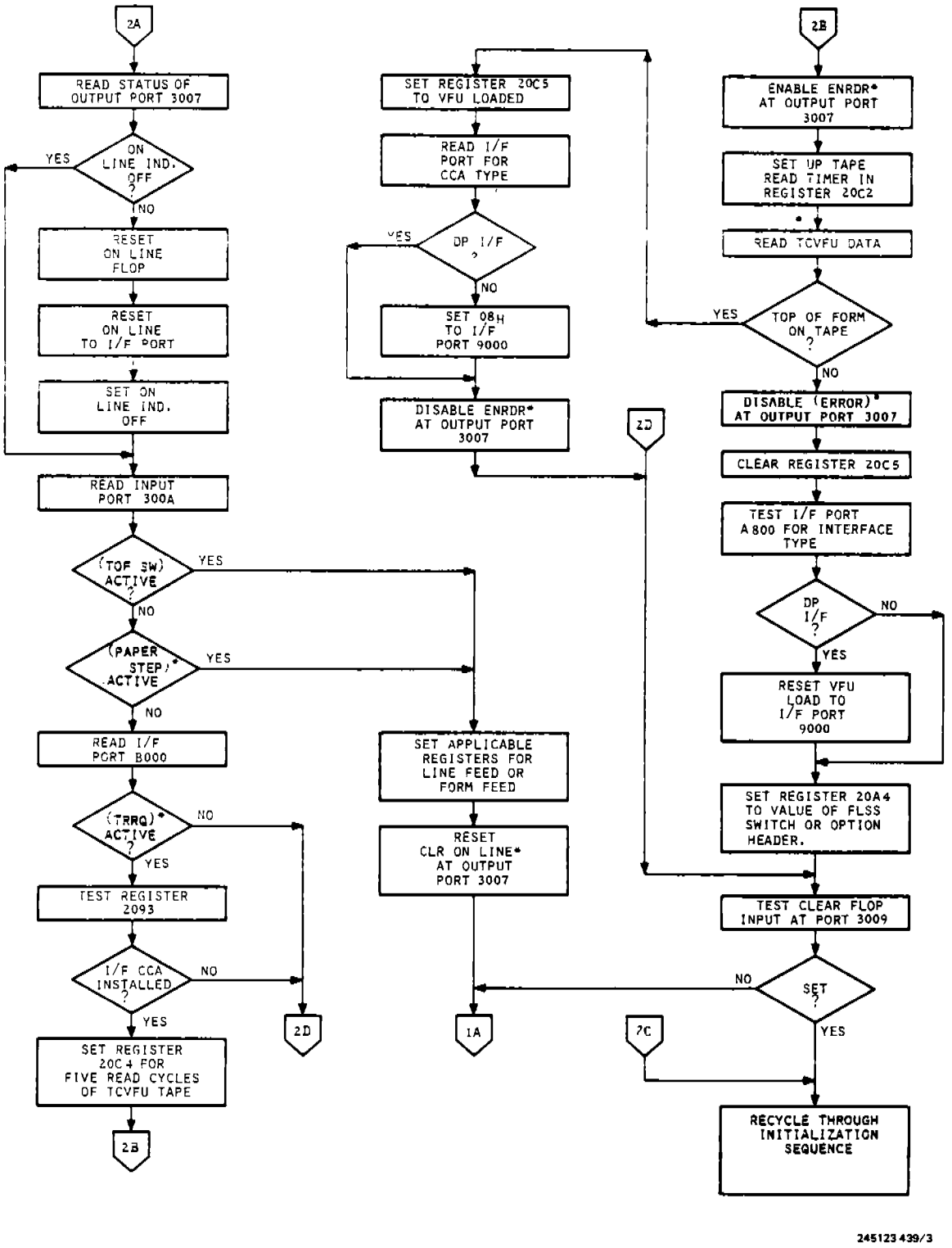



Figure 2-30C. Operating Status Verification Flow Diagram

## TABLE 2-14. INTERFACE PORT DEVICE SELECTION

| Address Bit Configuration | | | | | | | | | | | | | | | | Chip Select Signal | Enable Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 1 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CS1* | Read and Write to VFU/ Print |
| 1 | 0 | 0 | 0 | 1 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CS2* | Read last address counter value |
| 1 | 0 | 0 | 1 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CS3* | Interface Status Latch |
| 1 | 0 | 0 | 1 | 1 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CS4* | TCVFU Driver (upper byte) |
| 1 | 0 | 1 | 0 | 0 | NOT USED | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CS5* | Not Used |
| 1 | 0 | 1 | 0 | 1 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CS6* | Interface Status Latch |
| 1 | 0 | 1 | 1 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CS7* | TCVFU Driver (lower byte) |
| 1 | 0 | 1 | 1 | 1 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CS8* | Option Switch Driver |

1 = Logic High State
0 = Logic Low State
* = Active in Logic Low State. A Read or Write command must be active.

Address bit A15 is inverted on the Processor CCA to generate active low pulse A15* which is used to enable interface port transceiver U28. With U28 enabled, the CPU and Control Section controls the transfer of information between the internal D bus and the external DBUF bus.

Descriptions of the interaction of the various devices with the DBUF bus are provided in the applicable Interface CCA description.

a. Interface Port Address and DBUF Bit Assignments

The hexadecimal addresses of the various interface devices are sequentially listed below. Included are definitions for the bit assignment of each device.

1. Address $8800_H$ - VFU/Print Data Address Counter - An input latch which indicates the location in the I/F CCA VFU/Print Data Line Buffer where data is stored.

2. Address $9000_H$ - Interface Control Latch - The DBUF bit numbers, signal names, and functions are listed as follows:

| DBUF Bit No. | Signal | Function |
|---|---|---|
| 1 | LOAD BUFFER | Informs the Interface CCA to start loading the print buffer |
| 2 | READY | Informs the Interface CCA that the Processor CCA is ready to go on line or off line. |

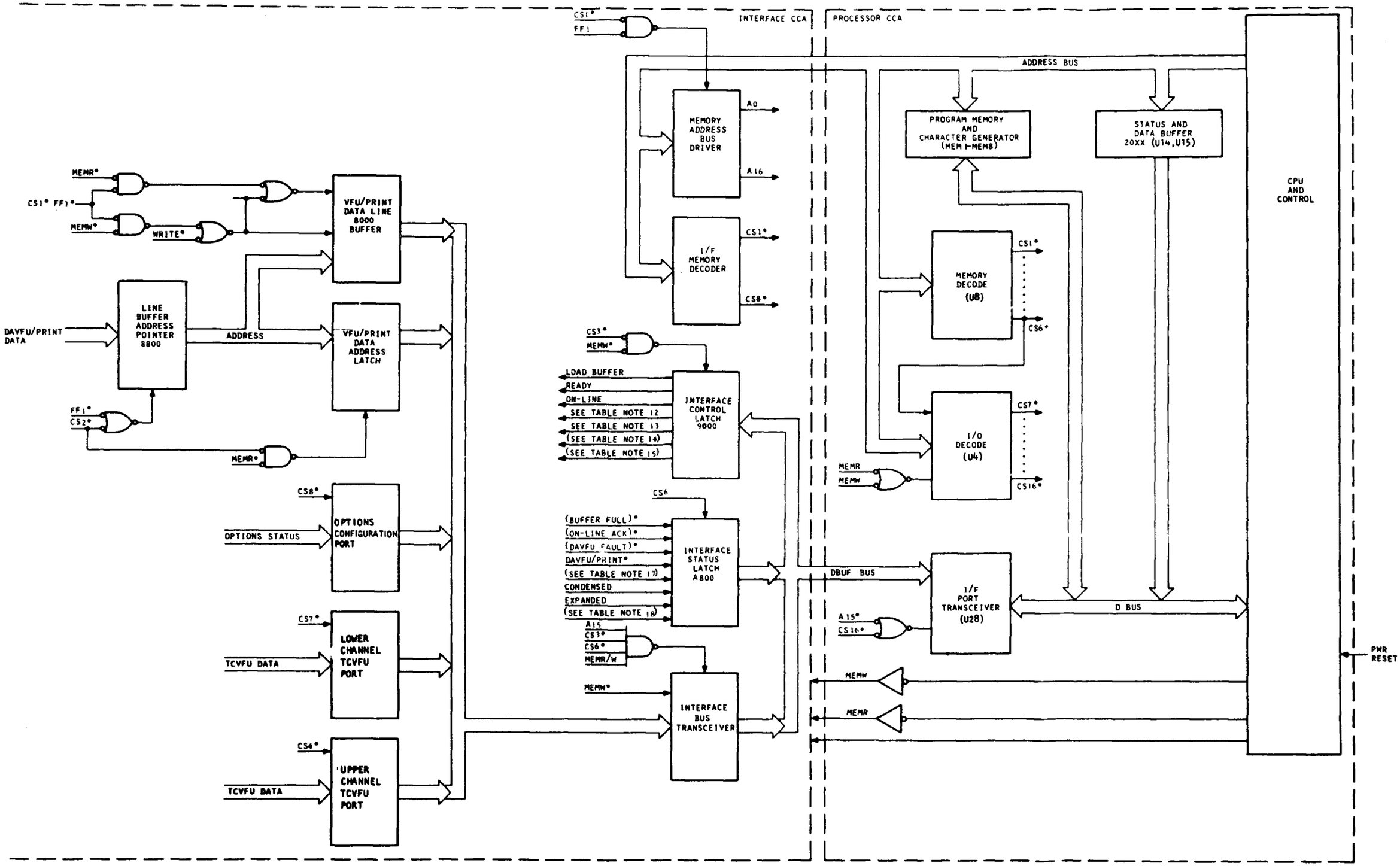



Figure 2-31. Processor CCA Interface Port Communications Functional Block Diagram

| DBUF Bit No. | Signal | Function |
|---|---|---|
| 3 | ON LINE | Informs the Interface CCA whether the Processor CCA is in the on line or off line mode. |
| 4 | TOP OF FORM (TOF) | Informs the Interface CCA that the Top of Form position has been detected. |
| 5 | BOTTOM OF FORM (BOF) | Informs the Interface CCA that the Bottom of Form position has been detected. |
| 6 | PAPER MOVING | Informs the Interface CCA that paper is moving. |
| 7 | CONDENSED | Informs the Interface CCA that the condensed 16 pitch switch is active. |
| 8 | PAPER EMPTY (PE) | Informs the interface CCA that the Paper Low Interlock is active. |

3. Address $A800_H$ - Interface Status - The DBUF bit numbers, signal names, and functions are listed as follows:

| DBUF Bit No. | Signal | Function |
|---|---|---|
| 1 | BUFFER FULL | Informs the Processor CCA that the Interface CCA has completed a load cycle. |
| 2 | ON LINE ACK | Acknowledges the ON LINE/OFF LINE status generated by the Processor CCA. |
| 3 | DAVFU FAULT | Informs the Processor CCA that the DAVFU load cycle has a fault, or that a parity error exists. |
| 4 | DAVFU/PRINT* | Informs the Processor CCA whether the loaded information is DAVFU or print data. |
| 5 | SAT* | Informs the Processor CCA that the Interface CCA is selected (DPC Centronics-Compatible Interface Only). |
| 6 | CONDENSED | Informs the Processor CCA that the line loaded was transmitted with a CONDENSED code. |
| 7 | EXPANDED | Informs the Processor CCA that the line loaded was transmitted with an EXPANDED code. |
| 8 | DPC/CENT* | Informs the Processor CCA whether the Dataproducts Centronics-Compatible Interface is present in the printer. |

4. Address $B000_H$ - TCVFU Status - The DBUF bit numbers, signal names, and functions are listed as follows:

| DBUF Bit No. | Signal | Function |
|---|---|---|
| 1 | CH1 | Channel 1 of the TCVFU Reader |
| 2 | CH2 | Channel 2 of the TCVFU Reader |
| 3 | CH3 | Channel 3 of the TCVFU Reader |
| 4 | CH4 | Channel 4 of the TCVFU Reader |
| 5 | CH5 | Channel 5 of the TCVFU Reader |
| 6 | CH6 | Channel 6 of the TCVFU Reader |
| 7 | TRRQ* | Informs the Processor CCA of the status of the TCVFU Reader switch. |
| 8 | CH13 | TCVFU Reader strobe (sprocket) pulse. |

5. Address $B800_H$ - Header Status - The DBUF bit numbers, signal names, and functions are listed as follows:

| DBUF Bit No. | Signal | Function |
|---|---|---|
| 1 | CONDENSED EN* | Informs the Processor CCA that condensed print option is enabled. |
| 2 | AUTO LF EN* | Informs the Processor CCA that automatic line feed option is enabled. |
| 3 | DAVFU EN* | Informs the Processor CCA that the DAVFU option is enabled. |
| 4 | PERF SKIP #1* | These two bits are coded to indicate to the Processor CCA the amount of perforation skipover required, as follows: |
| 5 | PERF SKIP #2* | |

| Perf. Skip #1 | Perf. Skip #2 | Lines of Skipover |
|---|---|---|
| 0 | 0 | 3 |
| 0 | 1 | 4 |
| 1 | 0 | 6 |
| 1 | 1 | 0 |

| DBUF Bit No. | Signal | Function |
|---|---|---|
| 6 | 11/12* FORM EN | Conditions the Processor CCA to compute number of print lines on form based on either 11 (high) or 12 (low) inches. |
| 7 | PLOT EN | Not Used. |
| 8 | EXPANDED DIS* | Informs Processor CCA that expanded print option is disabled. |

b. Data Transfer

On completion of the Operating Status Verification sequence, LOAD BUFFER is set to Interface Port $9000_H$, and Registers 20C2 and 20C3 are set to 350 milliseconds. If BUFFER FULL* does not become active within the 350 millisecond load window, the I/O ports will be enabled to perform a shuttle stop operation.

When BUFFER FULL* becomes active, the value of Interface port $8800_H$ is read to determine the location in the Interface VFU/PRINT data line buffer where the termination code is stored.

NOTE

For printers configured with a Serial Interface CCA, Location 00 of the VFU/PRINT data line buffer is read to determine the location of the termination code.

During the time that data is read from Interface Port $8000_H$, LOAD BUFFER is disabled at Interface Port $9000_H$.

2.5.4 I/O Port Communication and Control (Figures 2-32 and 2-33)

The Processor CCA uses nine I/O port devices to communicate with the control panel and the Wire Driver and Motor Driver CCAs. As shown in the functional flow block diagram, figures 2-32 and 2-33, each port device is assigned a hexadecimal address which corresponds to an eight-bit register location in the Status and Data Register (see paragraph 2.5.2).

a. I/O Port Enable Codes

The CPU and Control Section communicates with each I/O port device by issuing a unique 16-bit address code which is decoded into an enabling chip select signal as listed in table 2-12. The communication path between the CPU and Control Section and the individual I/O port device is completed by U27, which operates in either the transmit or receive code.

Table 2-15 lists the chip select signals, their address bus bit configurations, and enable functions.

TABLE 2-15. I/O DEVICE ENABLE SIGNALS

| Address Bit Configuration | | | | | | | | | | | | | | | | Chip Select Signal | Enable Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0 | 0 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | X | X | CS5* | Status and Data Register U14, U15 |
| 0 | 0 | 1 | 1 | 0 | X | X | X | X | X | X | X | X | X | X | X | CS6* | I/O Port Transceiver U27 |
| 0 | 0 | 1 | 1 | 0 | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 | CS7* | Output Port U24** |
| 0 | 0 | 1 | 1 | 0 | X | X | X | X | X | X | X | 0 | 0 | 0 | 1 | CS8* | Output Port U25 |
| 0 | 0 | 1 | 1 | 0 | X | X | X | X | X | X | X | 0 | 0 | 1 | 0 | CS9* | Output Port U30** |
| 0 | 0 | 1 | 1 | 0 | X | X | X | X | X | X | X | 0 | 0 | 1 | 1 | CS10* | Output Port U29** |
| 0 | 0 | 1 | 1 | 0 | X | X | X | X | X | X | X | 0 | 1 | 0 | 0 | CS11* | Input Port U26 |
| 0 | 0 | 1 | 1 | 0 | X | X | X | X | X | X | X | 0 | 1 | 0 | 1 | CS12* | Input Port U31 |
| 0 | 0 | 1 | 1 | 0 | X | X | X | X | X | X | X | 0 | 1 | 1 | 0 | CS13* | Input Port U21 |
| 0 | 0 | 1 | 1 | 0 | X | X | X | X | X | X | X | 0 | 1 | 1 | 1 | CS14* | Output Port U22 |
| 0 | 0 | 1 | 1 | 0 | X | X | X | X | X | X | X | 1 | 0 | 0 | 0 | CS15* | Output Port U23 |
| 0 | 0 | 1 | 1 | 0 | X | X | X | X | X | X | X | 1 | 0 | 1 | 0 | CS16* | Interface Port Transceiver U28 |
| 1 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | | Interface CCA Enable |

1 = Logic High State
0 = Logic Low State
** M200 Only
X = Don't Care
* = Active when in the Low State

I/O Port transceiver U27 is enabled when CS6*, the output from memory decoder U28, is in the logic low state. The transmit/receive mode is controlled by the logic state of the signal MEMR* output from the CPU and Control Section. As shown in figure 2-32, the CS6* pulse is used to enable the I/O port address decoder. The I/O port address decoder U40 receives the decoded four least significant bits of the address bus and outputs a unique decoded I/O device enable chip select signal pulse (CS7* - CS15*). The CS16* output from the I/O decoder is ORed with address bit A15*, which enables the interface port transceiver U28 when interface port communication is performed.

To control paper advance, ribbon advance, shuttle movement, and print wire firing, the CPU and Control Section will issue a unique address for the applicable I/O port device. The address decoder, enabled by either a read MEMR* or a write MEMW* command, will decode the address into a specific chip select pulse. When the various I/O port devices are enabled, the CPU and Control Section can manipulate the outputs and read the input when controlling any of the above mentioned functions.

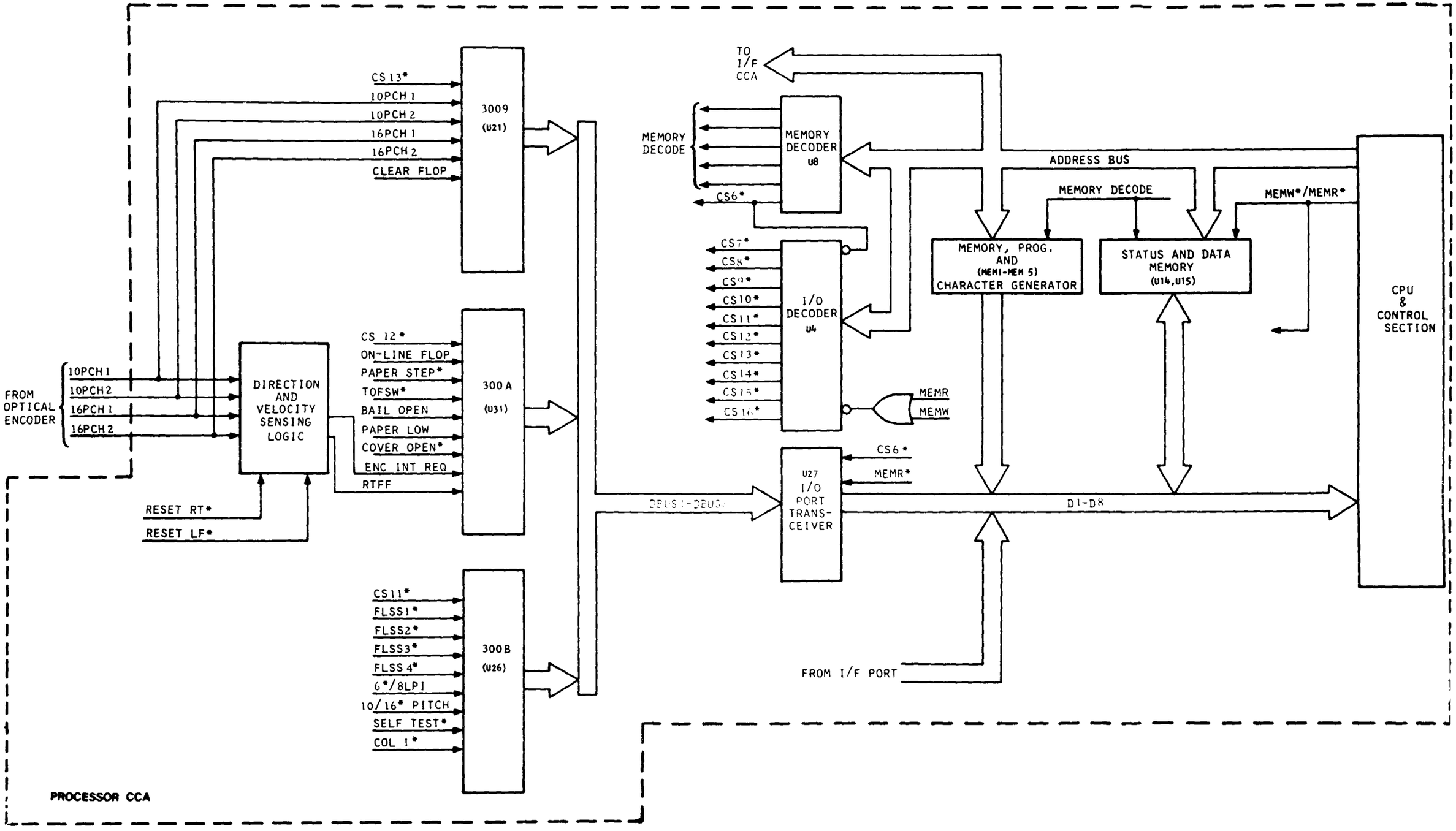



Figure 2-32. Input Ports Functional Block Diagram

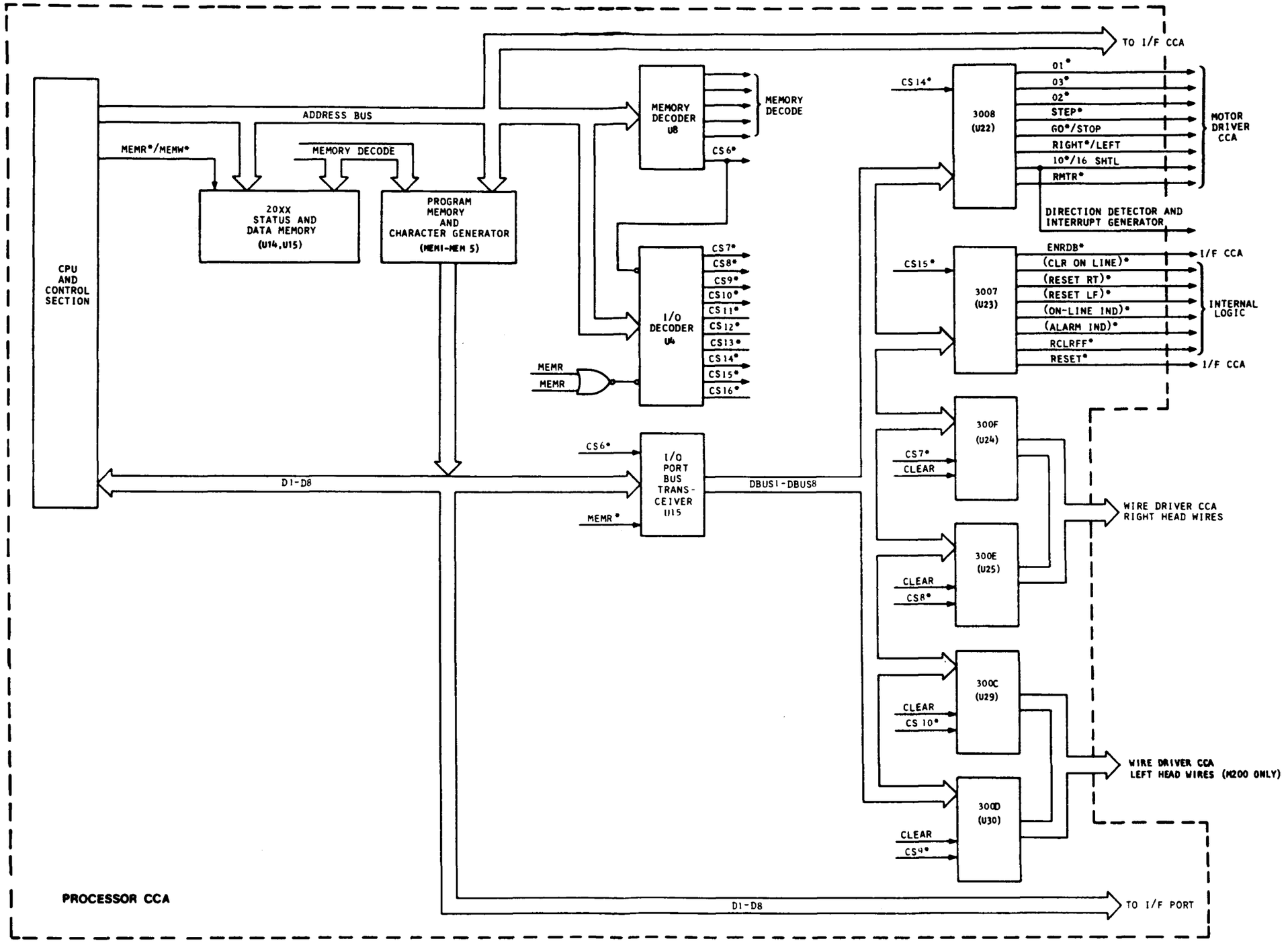



Figure 2-33. Output Ports Functional Block Diagram

b. I/O Port Signal Definitions

The hexadecimal addresses of the various I/O port devices are sequentially listed below. Included are definitions for the assignment of each bit interconnected with the DBUS.

1. Address $3007_H$

| DBUS Bit | Signal | Definition |
|---|---|---|
| 8 | RESET* | Used to reset the Interface CCA. |
| 7 | RCLRFF* | Used to clear the right clear flip-flop. |
| 6 | ALARM IND* | Used to turn the ALARM/CLEAR switch indicator lamp on or off. |
| 5 | ON LINE IND* | Used to turn the ON/OFF LINE indicator on or off. |
| 4 | RESET LF* | Used to clear the left sensing flip-flop. |
| 3 | RESET RF* | Used to clear the right sensing flip-flop. |
| 2 | ENRDR* | Used to enable the TCVFU reader. |
| 1 | CLR ON LINE* | Used to clear the on line flip-flop. |

2. Address $3008_H$

| DBUS Bit | Signal | Definition |
|---|---|---|
| 8 | RMTR* | Used to enable the ribbon advance motor. |
| 7 | 10/16 SHTL* | Used to select shuttle travel velocity which corresponds to print density (pitch). |
| 6 | RIGHT/LEFT* | Indicates the direction in which the shuttle will move. |
| 5 | GO/STOP* | Indicates whether the shuttle will stop or go. |
| 4 | STEP | Used to apply power to the paper stepper motor. |
| 3 | 01 1- 03* | Paper step phase signals used to move paper as follows: |

| $0_3$ | $0_2$ | $0_1$ | Paper Moved |
|---|---|---|---|
| 0 | 1 | 1 | One Step |
| 1 | 1 | 0 | One Step |
| 1 | 0 | 1 | One Step |
| 0 | 1 | 1 | One Step |

3. Address $3009_H$

| DBUS Bit | Signal | Definition |
|---|---|---|
| 5 | CLRFF | Indicates the state of the clear flip-flop. |
| 4 | 16PHC2 | Indicates the data output from the optical encoder. |
| 3 | 16PCH1 | Indicates the data output from the optical encoder. |
| 2 | 10PCH2 | Indicates the data output from the optical encoder. |
| 1 | 10PCH1 | Indicates the data output from the optical encoder. |

4. Address $300A_H$

| DBUS Bit | Signal | Definition |
|---|---|---|
| 8 | RTFF | Right flip-flop used to indicate when the shuttle is moving in the right (active high) or left (active low) direction. |
| 7 | ENCS | Used to indicate an encoder mark (the logical ORed outputs of the right and left flip-flops). |
| 6 | COVER OPEN* | Indicates when the cover is open. |
| 5 | PAPER LOW | Indicates when the printer is out of paper. |
| 4 | BAIL OPEN | Indicates when the bail is open. |
| 3 | TOFSW* | Indicates the position of the TOP OF FORM switch. |
| 2 | PAPER STEP* | Indicates the position of the PAPER STEP switch. |
| 1 | ON LINE FLOP | Indicate the status of the on line flip-flop. |

5. Address $300B_H$

| DBUS Bit | Signal | Definition |
|---|---|---|
| 8 | COL 1* | Column 1 sensor - used to indicate that the shuttle position is right of column 1. |
| 7 | SELF TEST* | Indicates the position of the TEST switch. |
| 6 | 10/16 PITCH* | Indicates the position of the horizontal pitch switch. |
| 5 | 6/8 LPI* | Indicates the position of the vertical pitch switch. |
| 4-1 | FLSS4* to FLSS1* | Indicates the position of the forms length switch as follows: |

| FLSS4 | FLSS3 | FLSS2 | FLSS1 | LPI |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 11 |
| 0 | 0 | 0 | 1 | 3 |
| 0 | 0 | 1 | 0 | 3½ |
| 0 | 0 | 1 | 1 | 4 |
| 0 | 1 | 0 | 0 | 5½ |
| 0 | 1 | 0 | 1 | 6 |
| 0 | 1 | 1 | 0 | 7 |
| 0 | 1 | 1 | 1 | 8 |
| 1 | 0 | 0 | 0 | 8½ |
| 1 | 0 | 0 | 1 | 11 |
| 1 | 0 | 1 | 0 | 12 |
| 1 | 0 | 1 | 1 | 14 |
| 1 | - | 0 | 0 | 11 |
| 1 | 1 | 1 | 0 | 11 |
| 1 | 1 | 1 | 1 | 11 |

6. Address $300C_H$

| DBUS Bit | Signal | Definition |
|---|---|---|
| 8-1 | 7L* to 1L* | Individual print wire control signals used to drive the left column print wires.** |

7. Address $300D_H$

| DBUS Bit | Signal | Definition |
|---|---|---|
| 8-1 | 7L* to 1L* | Individual print wire control signals used to drive the left column print wires.** |

8. Address $300E_H$

| DBUS Bit | Signal | Definition |
|---|---|---|
| 8-1 | 7R* to 1R* | Individual print wire control signals used to drive the right column print wires. |

9. Address $300F_H$

| DBUS Bit | Signal | Definition |
|---|---|---|
| 8-1 | 7R* to 1R* | Individual print wire control signals used to drive the right column print wires. |

** M200 Only

c. Print Head Shuttle Control (Figures 2-32, 2-33, and 2-34)

The print head is transported across the print station by a belt-driven shuttle mechanism assembly. The shuttle mechanism drive belt is coupled to the shaft of a velocity controlled DC motor. The Processor CCA uses output ports $3008_H$ (see figure 2-33) to control the motor rotation rate and direction. Output port $3007_H$ is used to initialize the internal logic, which detects shuttle rate. Input ports $3009_H$, $300A_H$, and $300B_H$ (see figure 2-32) are used to input shuttle-to-platen data, velocity rate, print wire firing of synchronous pulses, and direction of shuttle travel.

To initiate shuttle motion for a given direction and to control the travel velocity, the Processor CCA uses RIGHT*/LEFT and 10*/16 at output port $3008_H$ (see figure 2-33) to communicate with the Motor Driver CCA. Signal 10*/16 is also input at port $300B_H$ and is used by the Processor CCA to compute end zone reference points for reversing shuttle motion. Signals RESET RT* and RESET LF* at output port $3007_H$ (see figure 2-33) are used to clear the velocity and direction sensing logic internal to the Processor CCA.

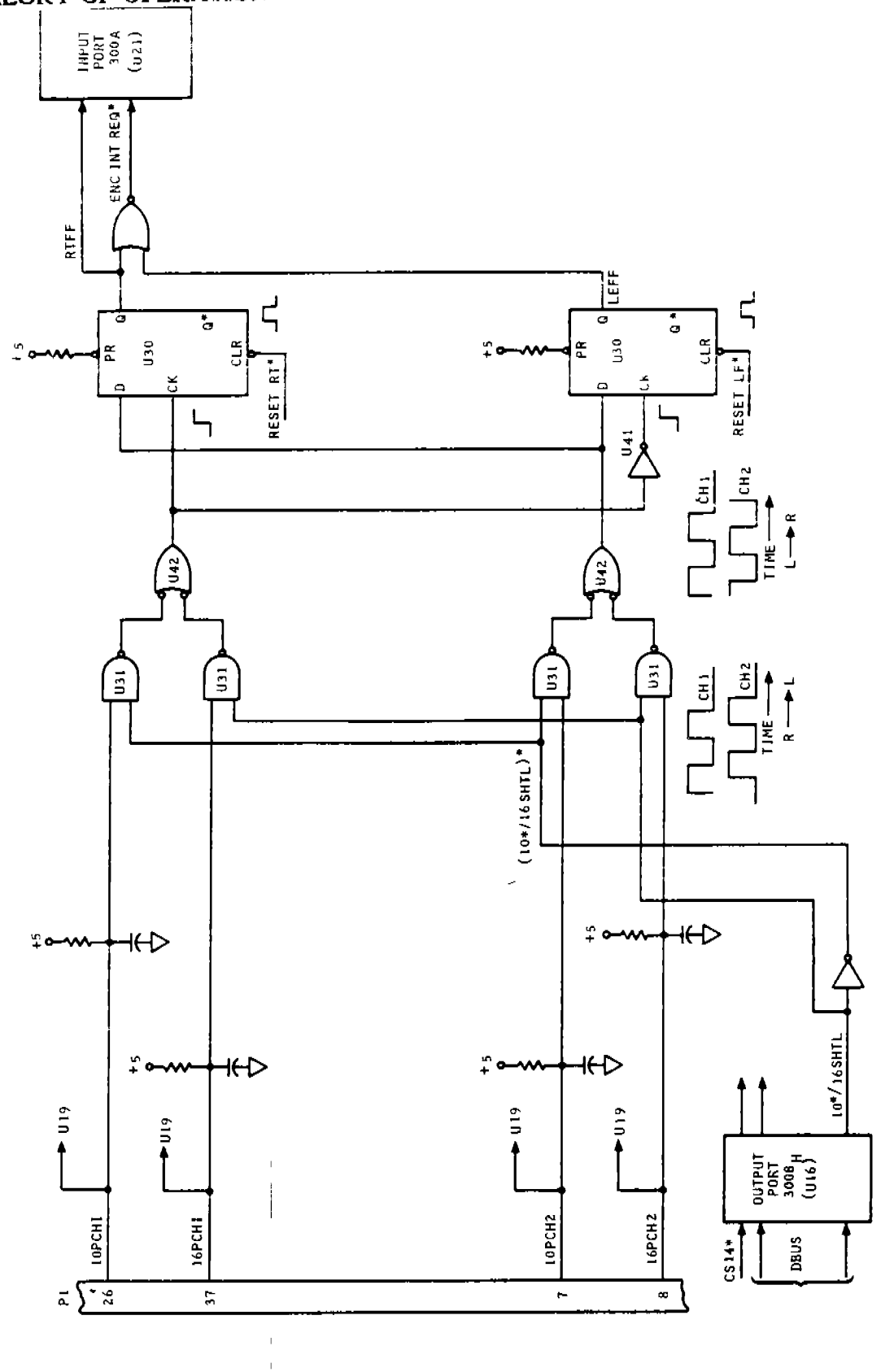



Figure 2-34. Direction and Velocity Detection Logic

When shuttle motion is in progress, the optical encoder assembly transfers a pulse train to the Processor CCA that indicates shuttle velocity. The pulse train (10PCH1, 10PCH2, or 16PCH1, 16PCH2) is input onto the Processor CCA at port $3009_H$ (see figure 2-32) and to the Direction and Velocity logic network (see figure 2-34). Encoder inputs at $3009_H$ are used to detect direction of travel when shuttle parking is to be performed (refer to subparagraph 1).

The encoder inputs to the Direction and Velocity Sensing Network (see figure 4-31) are used to develop the CPU and Control Section interrupt signals ENC INT REQ* and right/left status pulse RTFF. These signals are transferred to input port $300A_H$ and are used to synchronize shuttle velocity, and direction with print wire firing.

The 10/16* PITCH and COL 1* signals at input port $300B_H$ (see figure 2-34) are used to determine the switch setting for shuttle velocity and to detect when the shuttle is at the column one position near the left end frame.

To control shuttle movement, the Processor CCA will first park the shuttle at a referenced home position and initialize internal control logic. Next, an active signal BUFFER FULL* from the interface port will cause the CPU and Control Section to seek current shuttle position and move the shuttle to the nearest print position.

1. Parking the Shuttle at the Home Position (Figures 2-32, 2-33) and 4-13) - Parking the shuttle at the home position is performed under any of the following conditions:

   (a) When the POWER switch is reset, or

   (b) When a change occurs in the state of the ON LINE switch.

   The shuttle is stopped in place:

   (a) When the shuttle velocity and pitch settings do not agree.

   (b) When a STOP command is generated because of a malfunction.

When shuttle parking is to be performed, the CPU and Control Section will first initialize a no-shuttle motion timer (Status and Data Registers $20C2_H$ and $20C3_H$). Next, the interrupt input signal ENC INT REQ* is disabled. The status of outport port $3008_H$ is then tested to determine the logic state of GO*/STOP. If GO*/STOP is in the low state, input port $300B_H$ is then enabled to read the status of COL 1*. If the COL 1* input is at the high state, output port $3008_H$ is enabled. RIGHT*/LEFT is forced to the high state, and the no-motion timer is decremented until COL 1* switches to the low state. If the timer

should time out before COL 1* switches low, all the control signals interfacing the motor driver power circuits will be disabled. When COL 1* switches to the low state, input port $3009_H$ is enabled and the 10 PCH2 input is monitored until a low-to-high transition occurs. The low-to-high transition will cause the CPU and Control Section to force the RIGHT*/LEFT output of port $3008_H$ low.

When the status of GO*/STOP indicates a high state, the state of COL 1* is input. If COL 1* is in the high state, the RIGHT*/LEFT output of port $3008_H$ is forced high, the status is stored in the Status and Data Register, and the motion timer is decremented until COL 1* switches low. If the timer should time out before COL 1* switches low, power to all drive motors will be disabled.

A low transition of COL 1* will cause the RIGHT*/LEFT output of port $300B_H$ (see figure 2-33) to switch low. The low state of RIGHT*/LEFT will cause the 10PCH2 input to port $300B_H$ to be monitored for a low-to high transition. When 10PCH2 switches high, implying that the shuttle is now moving to the right from the left end frame, the state of 10/16* at input port $300B_H$ is tested to determine travel velocity. The state of this signal will cause a set or reset state of 10*/16 SHTL at output port $3008_H$ (see figure 4-31). The status of 10*/16, indicating shuttle velocity, is stored in the applicable Status and Data Register. This velocity will remain fixed and used as the reference speed for print wire firing unless the print format option is changed.

The COL 1* input is then tested for a low-to-high transition (shuttle leaving the column one position). If the shuttle motion timer (Status and Data Registers 20C2 and 20C3) should zero out before COL 1* changes state, power to all motors is disabled. When COL 1* switches high, the RESET LF* and RESET RT* outputs from port $3007_H$ (see figure 2-33) are clocked into flip-flop U11 (see figure 2-34) to clear the LEFF and RTFF outputs from Status and Data Register 2090 each time an interrupt is generated. LEFF is ORed with RTFF to generate interrupt signal ENC INT REQ* for each dot column the shuttle traverses.

After clearing the LEFF and RTFF flip-flops, the dot column counter is cleared to zero (Status and Data Register 2090), and simultaneously, a 17D is loaded into the character column counter (Status and Data Register 2091). At the same time, signal ENC INT REQ* is enabled for counting dot columns, and as the shuttle is moving, every tenth RTFF will increment or decrement the character column counter. With the shuttle moving to the right from the left end frame, the character column counter will be incremented. When a count of 36D is reached, the RIGHT*/LEFT output of port $3008_H$ (see figure 2-33) will switch to the high state, causing the shuttle to reverse direction toward the left. The 10PCH2 input at port $3009_H$ is then monitored for a low-to-high transition. When the transition is detected, the CPU and Control Section will enable output port $3008_H$ (see figure 2-32) and set GO*/STOP to the high state. When in the high state, GO*/STOP will disable power to the shuttle motor drive circuit on the Motor Driver CCA. The shuttle is then parked at the home position, and the shuttle control logic is initialized.

2. Velocity Direction Control (Figure 2-34) - The standard printer has a velocity of 34 inches per second (IPS), which is the reference velocity

for printing at ten characters per inch (CPI). Printers configured with the optional 10/16 PITCH switch have a velocity of 20.4 IPS for the 16 pitch setting (16 CPI). When the Condensed Print option is enabled, shuttle velocity is 20.4 IPS, and is 34 IPS when the Expanded Print option is enabled. Either velocity is maintained for each print line unless the 10/16 PITCH switch setting is changed or unless a change is detected in the logic states of the CONDENSED and EXPANDED bits at interface status latch $A800_H$ (see figure 2-31).

Referring to figure 2-34, the logic state of 10*/16 SHTL output from port $3008_H$ is set during shuttle parking and initialization. The 10*/16 SHTL signal is NANDed with encoder output signals 10PCH1 and 10PCH2. The logic state of 10*/16 SHTL determines which encoder output will be analyzed for shuttle direction.

The frequency of either the 10 pitch or 16 pitch pulse train will specify the shuttle travel velocity. A pulse is generated for each instance that the encoder assembly, attached to the shuttle, intersects an imaginary dot column position on the platen. When shuttle motion is in progress, to perform a print operation, the encoder outputs over channel 1 are used to clock the channel 2 pulse train through flip-flop U11. The right sensing output (RTFF) and left sensing output (LEFF) are ORed to generate the CPU and Control Section interrupt signal ENC INT REQ*.

Signal ENC INT REQ* is generated every 294 microseconds (M200 only), which the CPU and Control Section uses as an index for synchronizing print wire firing. Signal RTFF is the dot column count, and depending on shuttle travel direction, will increment or decrement Status and Data Register $2090_H$ (dot column counter). Every tenth increment or decrement of the dot column count will cause an increment or decrement of the character column count in Status and Data Register $2091_H$ (character column counter). The CPU and Control Section reads the content of these registers to determine shuttle horizontal position.

To compute the shuttle's travel direction, the leading edge of pulse 10PCH1 or 16PCH1 is used as a reference to analyze the pulse transitions received on channel 2. If the pulse on channel 2 is high when the leading edge of channel 1 is switched from low to high, the LEFF output is cleared and RTFF output from U11 will be set. This condition indicates that the shuttle is traveling in the direction of left end frame. This condition will cause the RTFF output to be cleared and the LEFF to be set.

The direction in which the shuttle travels to perform a print operation depends upon the location of the print characters stored at I/F port $8800_H$ (see figure 2-32). When the status of I/F port $A800_H$ indicates that the buffer is full and contains print data, I/F port $8800_H$ is interrogated for the presence of first and last print characters. The CPU and Control Section translates this data into start of line (SOL) and end of line (EOL) and stores the computed values in the allocated Status and Data Registers. The CPU and Control Section compares the contents of the character column register with the SOL and EOL registers to determine shuttle position with respect to character print position. The computed value logic state of RIGHT*/LEFT controls the operation of the reversing amplifier located on the Wire

Driver CCA. The reversing amplifier will cause the shuttle mechanism drive motor to rotate in the correct direction. When in motion, the encoder will output pulse train 10PCH or 16PCH, which is analyzed for direction and velocity.

When the shuttle mechanism is computed to be at the last dot column of the last character column to be printed, the CPU and Control Section will set or reset the RIGHT*/LEFT output of Output Port $3008_H$, reversing the direction of motion of the shuttle drive motor. During the time period when the shuttle mechanism is turning around (60 milliseconds maximum, if the velocity is 20.4 inches per second, or 100 milliseconds if the velocity is 34 inches per second) the CPU and Control Section enables Interface Port Transceiver U28 and sets LOAD BUFFER to interface control latch $9000_H$ (see figure 2-32). If, during the turn-around time Interface Port $A800_H$ responds with a buffer full condition (BUFFER FULL* active when low), Interface Port $8000_H$ (see figure 2-32) is again interrogated for start of line and end of line data. (During shuttle turn-around time, output port $3008_H$ is used to step paper.)

d. Print Wire Firing, M200 Printer

The print function controls the information output to the print head. Printing is performed by accessing the ASCII-coded character from Interface Port 8800 and converting the data into an address to access the character. This 8-bit address is used to fire a wire column. Four internal counters are used to keep track of the position of the left and right wires. These counters are CCCL, DCCL and CCCR, DCCR respectively, and are used with the ASCII character code to access the character generator. Updating of the internal counters with each encoder mark keeps track of the print head position.

The character generator is divided into two parts. One part is addressed for the right wires, and the other for the left wires. The address which accesses the character generator is made up of the dot column counter (DCCR for the right wire section; DCCL for the left wire section) and the ASCII character code. The address selects one of eight bytes of data for a particular character. The selected byte will then be used to turn on any wire of the vertical wire column (where the uppermost wire is the least significant bit of the addressed byte from the character generator). The three low order bits of the dot column counter will access any of the eight bytes of data for a particular character. The sixth bit will be used to access either side of the character generator. The ASCII seven-bit code will be used to access any of the 128 characters in the character generator.

When printing at 10 or 16 characters per inch, the left and right wire banks are updated with information every 294 microseconds (M200 only), the period of one encoder mark. However, once a wire is fired, it must stay on for 355 $\pm 5$ microseconds. For this reason, output ports (registers) $300D_H$ and $300C_H$ are used for left wire data (M200 only). Output ports (registers) $300F_H$ and $300E_H$ are used for right wire data. Each pair of output ports are updated every 294 microseconds, with each individual output port of the left/right output port set being updated every 588 microseconds.

When printing at five characters per inch (expanded mode), the shuttle servo motor travels at the 10-characters-per-inch rate. However, every other encoder mark is skipped, and the same dot column information is printed

twice. This effectively expands the width of the character to 20 encoder marks. Of these, 14 are allotted for dot information and six for inter-character spacing. Since updating is only required on every other encoder mark, only one latched port to each pair is used: LB and RB.

e. Print Wire Firing, M120 Printer

As described earlier, the M200 and M120 printers use identical methods to obtain dot pattern information from the character generator. Therefore, the M120 printer also uses four internal counters, CCCL, DCCL, CCCR, and DCCR, to keep track of the print head position and access both halves of the character generator.

Once the character generator has been accessed, however, the dot patterns obtained from both halves of the character generator are applied to circuits controlling the right wire bank. (See sheet 5 of the Processor CCA logic diagram in Volume II of this manual.) Circuits that control the left wire bank in the M200 printer are always inactive in the M120 printer. These includes output ports $300D_H$ and $300C_H$ (CS10* and C59*).

The wire on time in the M120 printer, like in the M200 printer, is 355 $\pm$5 microseconds. Due to the longer period between dot times in the M120 printer, only one output port (register) is used. This register, U25, is controlled by chip select signal CS8*, register U24, controlled by chip select signal C57*, is always inactive in the M120 printer. Similarly, due to the longer period between dot times, only one-shot U6-5 is used, and one-shot U6-13 is always inactive in the M120 printer.

f. Ribbon Advance

Ribbon motion is initiated by the Processor CCA at the start of the shuttle or paper motion cycle through the ribbon drive system of the Motor Driver CCA.

g. Paper Advance Control (Figures 2-32 and 2-33)

Each time the printer is powered up, the CPU and Control Section will first initialize the paper advance controls. The CPU and Control Section first locks the paper feed stepping motor into phase one. This is accomplished by enabling U27 and setting the DBUS to a $B3_H$. The $B3_H$ output from U27 is placed on the DBUS, the CPU and Control Section enables Output Port $3008_H$, and the contents of the DBUS is output to the Motor Driver CCA. The low state of STEP* and 03* will energize the motor and start motor movement. After 4 milliseconds, the 03* signal is reset to high (inactive) and the 01* signal is set low (active), causing motor rotation to Phase 1. The STEP* signal is then reset high, de-energizing the motor in Phase 1. Upon completion of initialization of the stepping motor control circuitry, the CPU and Control Section loads Status and Data Register $20BD_H$ with the status of Output Port $3008_H$.

Next, the CPU and Control Section computes the Top of Form position from the total number of printable lines on the form and from the perforation skip code. To do this, the CPU and Control Section reads the applicable

bits of the option switches via driver $B800_H$ and I/F Port Transceiver (see figure 2-32). The CPU and Control Section detects the logic state of DBUF4 and DBUF5 to compute the number of lines to be skipped when performing perforation skipover, and stores the computed value into Status and Data Register $20A8_H$. If the printer is configured with the optional 6/8 CPI and Forms Length Select switches (FLSS), the CPU and Control section enables I/O Port Transceiver U27 and reads the content of Input Port $300B_H$ (U26). The logic state of DBUS5 establishes the line density (6 or 8 lines per inch), and is used to compute the total number of lines remaining on the form as specified by the logic state of DBUS1 through DBUS4.

The value of the FLSS setting is saved in Status and Data Register $20A5_H$, and loaded in Status and Data Register $20A4_H$, which is used as a counter for the number of print lines on the form.

In the standard printer, the CPU and Control Section enables both Interface Port Transceiver U20 and the Interface Bus Transceiver, and reads the logic state of DB6 output of the Option Switch Driver $B800_H$. The logic high or low status of DB6 is input to the Processor CCA, indicating that the printer is configured to handle 11-or 12-inch forms, and is saved in Status and Data Register $2045_H$. The 11-or 12-inch value is also loaded into Status and Data Register $20A4_H$, which is used as a counter for the number of print lines on the form. When Top of Form is reached, the CPU and Control Section will then set the DBUF4 line high true to the Interface Control Latch $9000_H$ (figure 2-32), and will store the status in Status and Data Register $20AD_H$.

After initializing the paper stepping motor control circuitry, and computing the perforation skip and/or forms length, the CPU and Control Section will then read the state of the applicable Status and Data Registers. These registers are re-initialized each time the CPU and Control Section is reset or a paper motion-related control panel switch setting is changed.

## 2.6 MOTOR DRIVER CCA (See Volume II)

The Motor Driver CCA contains the drive circuitry for the print head shuttle servo motor, the paper feed stepping motor, and the ribbon drive motor. The column 1 sensing amplifier U10 and motion suppress circuits are also included. Output of U10 is used as an input to the Processor CCA for print head shuttle reset positioning and as a marker for determining print head turn-around at the left end zone and start of print line at the left margin. The motion suppress circuit U10 detects the power on condition and prohibits accidental printing, shuttle motion, and paper incrementing during power on or off.

### 2.6.1 I/O Signal Definitions

Table 2-16 lists the I/O signals of the Motor Driver CCA and their functions.

**TABLE 2-16. MOTOR DRIVER CCA SIGNAL DEFINITIONS**

| Name | Function |
|---|---|
| STEP* | Low True. When true, this input enables full power to be applied to the stepping motor for the duration of stepping. |
| 01* | Low True. When true, this input turns to Phase 1 coil of stepping motor. |
| 02* | Low True. When true, this input turns on Phase 2 coil of stepping motor. |
| 03* | Low True. When true, this input turns on Phase 3 coil of stepping motor. |
| RM* | Low True. When true, this input turns on the ribbon motor. |
| 10 PCH1 | This input represents the 10 pitch encoder track, channel 1. |
| 16 PCH1 | This input represents the 16 pitch encoder track, channel 1. |
| 10*/16 SHTL | This input selects the correct encoder track for the shuttle servo motor. If low, 10 PCH1 is selected; if high, 16 PCH1 is selected. |
| R*/L | This input directs the motion of the shuttle. Low commands right motion, high commands left motion. This signal should change only when shuttle speed has settled or is at zero. |
| DET POS | This line represents the output of the "column one" sensor. (This is not a TTL signal.) |
| | (1) The asterisk implies function is alive in the low state. |
| | (2) Unless otherwise specified, all signals are TTL levels. |

### 2.6.2 Circuit Operation

This paragraph describes the shuttle servo motor, paper feed stepping motor, and ribbon drive motor operation.

#### a. Shuttle Servo Motor Control

A velocity-controlled DC motor, via a pulley and belt, drives the shuttle mechanism across the print station. The Processor CCA commands the servo motor with respect to GO/STOP, RIGHT/LEFT, and 16 PITCH (HI) 10 PITCH (LO) speed. An optical incremental encoder, mounted on the motor shaft, provides information for firing the print solenoids, and the same encoder signals are used to derive velocity information for the servo motor. A block diagram of the shuttle servo motor is shown in figure 2-35.

Referring to figure 4-12, SH 2, the correct track from the encoder is selected at gates U12-3, U11-3, and U11-11, and is fed to an edge detector circuit U4-8, U4-6, effectively doubling the encoder input frequency. The pulses at U4-6 trigger U5, a one-shot whose average positive DC output is compared with a negative DC reference voltage at R5. The error is amplified and carrier-filtered by low-pass filters U1 and U2. U3 is a "reversing" amplifier whose gain is -1 or +1, depending on the L/R signal. The output of U3, limited by CR4 and CR5, is next fed to a current drive switching power amplifier. This self-oscillating amplifier, consisting of U7, Q7, Q13, Q4, and Q15 drives the motor from the +21V and -21V supplies. Current feedback is obtained from R27, which is in series with the motor. The switching amplifier operates between 20 kHz and 25 kHz, to provide high power efficiency. Transistors Q3 and Q10 limit the current in the motor to avoid motor de-magnetization and excessive transistor current.

A re-triggerable one-shot at U9 is used to detect very slow movement or lack of shuttle motion if the GO command has been given. The one shot then times out, locks out further triggering and causes U6-13 to go low, grounding the bases of Q7 and Q13, thus shutting off the motor drive. U9 is reset only when the GO signal changes to STOP.

#### b. Paper Feed Stepping Motor Control (Figures 2-36 and 2-37)

A three-phase motor is used to drive the tractor assembly. For six lines per inch, the motor moves four steps to get one line of paper movement (see timing diagram, figure 2-36), and moves three steps per line for eight lines per inch. Normally, one phase winding is kept energized to produce a holding torque. For slewing, stepping is carried out continuously. See the timing diagram shown in figure 2-37.

Assume that Phase 3 is energized. In this phase, Q3* is low, turning on Q2, which then turns on Q1. Current flows through CR22, the Phase 3 winding, Q1, and into the -21V supply. In this manner, the holding torque is produced. To step the motor, STEP* goes low, turning on Q12, and resulting in turning on Q11, thus applying +21V to the motor common winding and back-biasing CR22. At the same time, Phase 3 is turned off and Phase 1 is turned on with the full supply voltage across it. Keeping signal STEP* low, the motor is stepped in

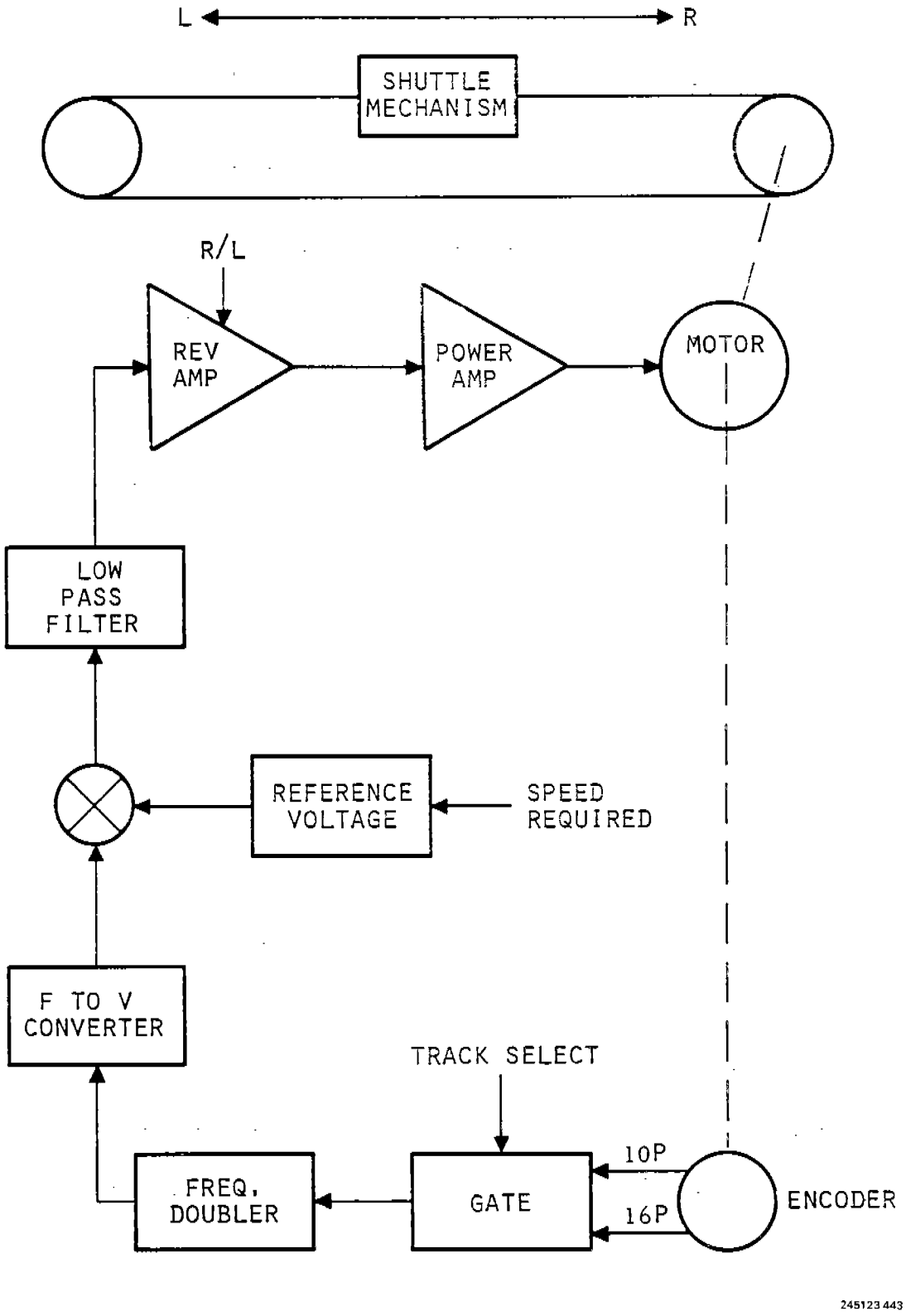
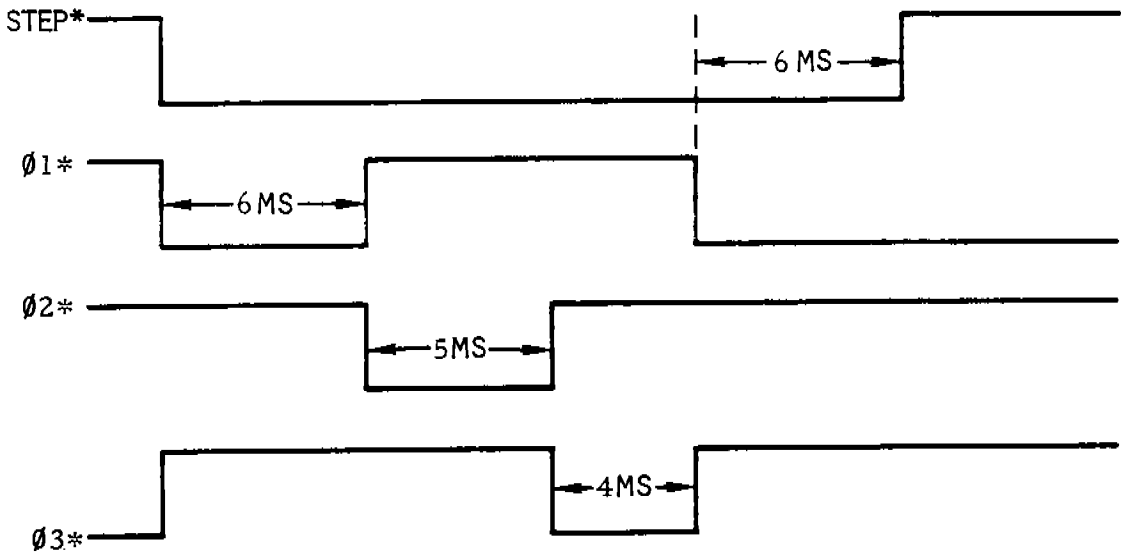


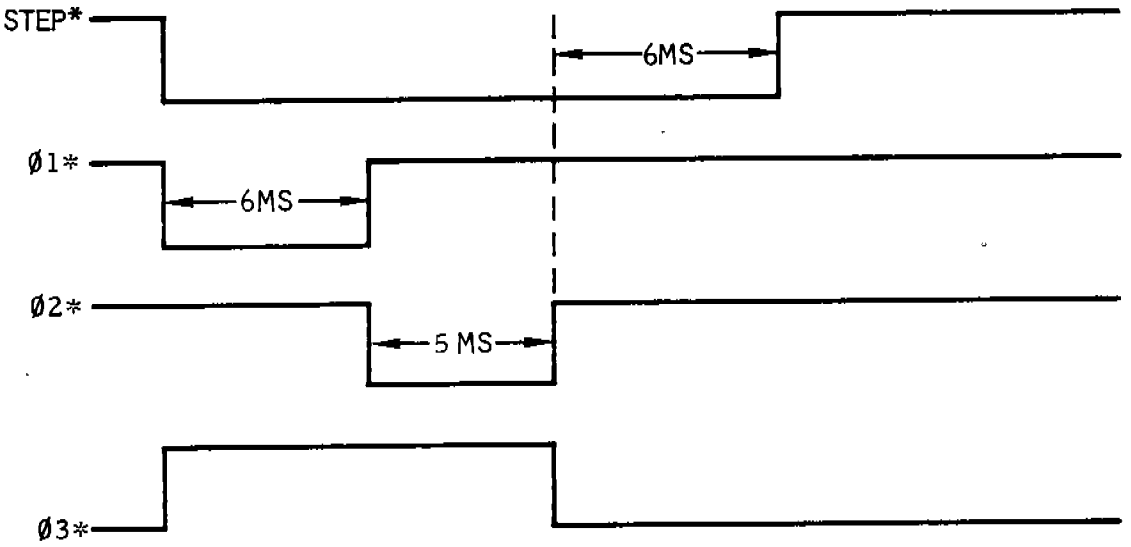

Figure 2-35. Shuttle Servo Motor Block Diagram

(A) FOR 6 LINES/INCH TOLERANCE: ± 100 µS




SEQUENCE: Ø3-Ø1-Ø2-Ø3-Ø1, Ø1-Ø2-Ø3-Ø1-Ø2, ETC.

(B) FOR 8 LINES/INCH




SEQUENCE: Ø3-Ø1-Ø2-Ø3-, Ø3-Ø1-Ø2-Ø3, ETC.

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Figure 2-36. Stepping Motor Input Waveforms (Line Step Mode)

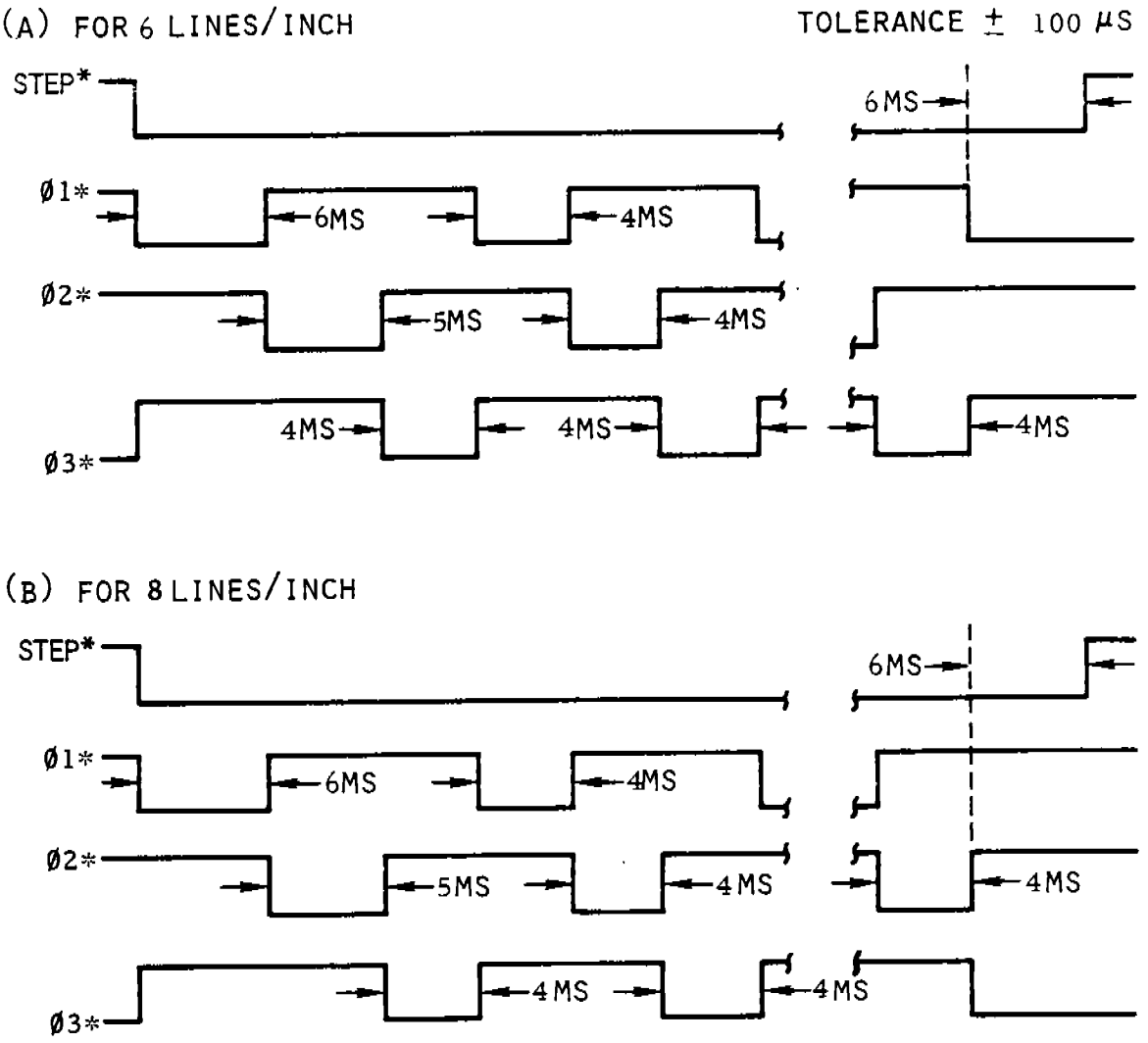



Figure 2-37. Stepping Motor Input Waveforms (Slew Mode)

sequence to Phase 1, Phase 2, Phase 3, etc. To terminate the stepping sequence, STEP* goes high, turning off Q11. One phase is still left on, via CR22 and the -21V supply.

c. Ribbon Motor Drive Control

When signal RMTR* goes low, Q14 is turned on, applying +21 volts to the ribbon drive motor, which drives the ribbon in the ribbon cassette via a gear-head. The ribbon motor is actuated only during printing.

1. Column One Sense Amplifier - U10-2 is a comparator which translates the analog detection of the photo-sense signal at pin 4 to a TTL signal at pin 2. This signal is used by the Processor CCA.

2. Motion Suppress Circuit - Two comparators, U10-1 and U10-14, are used to detect power on and power off, respectively. Their outputs are collector ORed to give inhibit signals via U10-13 to the print head drivers and the paper feed drivers, and via CR29, to the shuttle servo motor drive. This prevents accidental printing, shuttle motion, or paper incrementing during power on and power off.

## 2.7 WIRE DRIVER CCA (Figure 4-13, Volume II)

The Wire Driver CCA contains 14 solenoid drive circuits which interface the Processor CCA with the print head. Each solenoid drive circuit controls an associated print wire solenoid housed in the print head assembly.

NOTE

In the M120 printer, only seven solenoid drive circuits are active.

### 2.7.1 I/O Signal Definitions

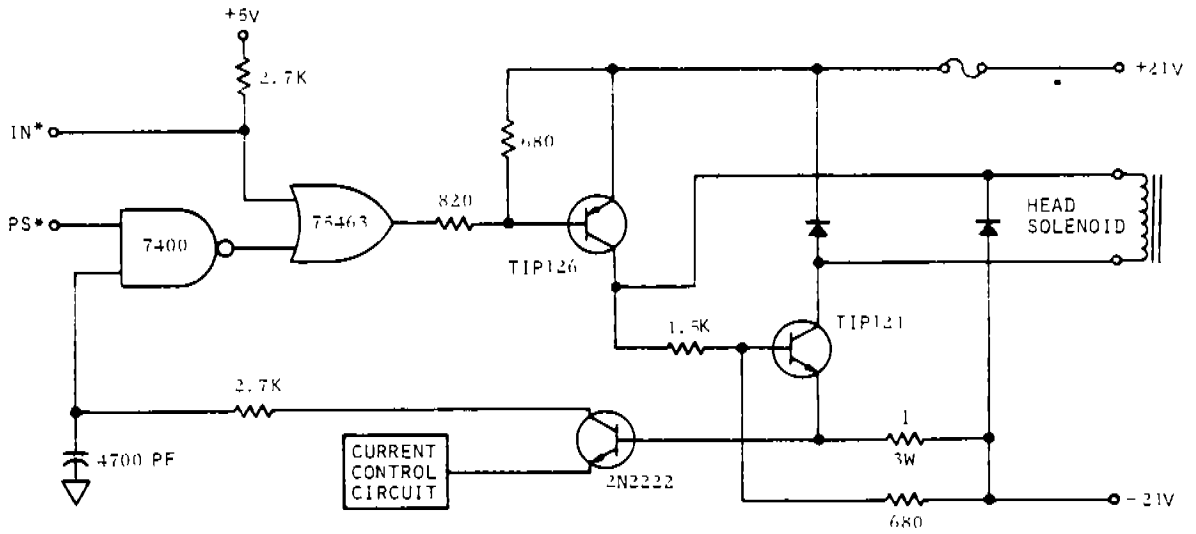
Table 2-17 lists the I/O signals of the Wire Driver CCA, and defines their functions.

**TABLE 2-17. WIRE DRIVER CCA I/O SIGNAL DEFINITIONS**

| Signal | Function |
|---|---|
| PS | (Print Suppress) - A TTL high true signal from the Motor Driver CCA that inhibits any spurious signal to the input of the wire drivers from inadvertently firing the print wires during printer power up or power down. |
| 1R* - 7R*<br>1L* - 7L* | Driver Input (Right/Left) - TTL low true signal from the Processor CCA that turns on the driver circuit. This signal should be low for not longer than 350 ±10 micro-seconds. |
| 1R1/1R0 -<br>7R1/7R0,<br>1L1/1L0 -<br>7L1/7L0 | Wire driver outputs are connected to the coils in the print head -- one on the inside (1) wire of each coil winding, and one on the outside (0) wire of each coil winding. At room temperature, the coil forms a load of approximately 1.45 ohms, 3.5 mHz. Nominally, the signals relative to each other; i.e., (1L1/1L0), remain at 0V when the driver is off. The waveform across the driver outputs is similar to that shown in figure 2-35 when the coil is activated. |

### 2.7.2 Circuit Operation (Figures 2-38 and 2-39)

Figure 2-38 shows a typical wire driver circuit. When the input signal is low, the output of OR gate (U13, U14, U17, U18, U21, U22, U24) goes low, turning on PNP transistor Q15-29. This causes current to flow through the transistor, which turns on NPN transistors Q30-Q4? The NPN transistor allows current to flow through the coil in the print head. As the current in the coil approaches a preset value, the voltage across the 1 -ohm sense resistor turns on the 2N2222 transistor. The voltage at the emitter of 2N2222 (current bias) determines the peak value of the current through the head coil. As the 2N2222 transistor is turned on, it discharges the 4700 pF capacitor at the input of NAND gate 7400.




ALL RESISTOR VALUES IN OHMS

**Figure 2-38. Typical Wire Driver Circuit**

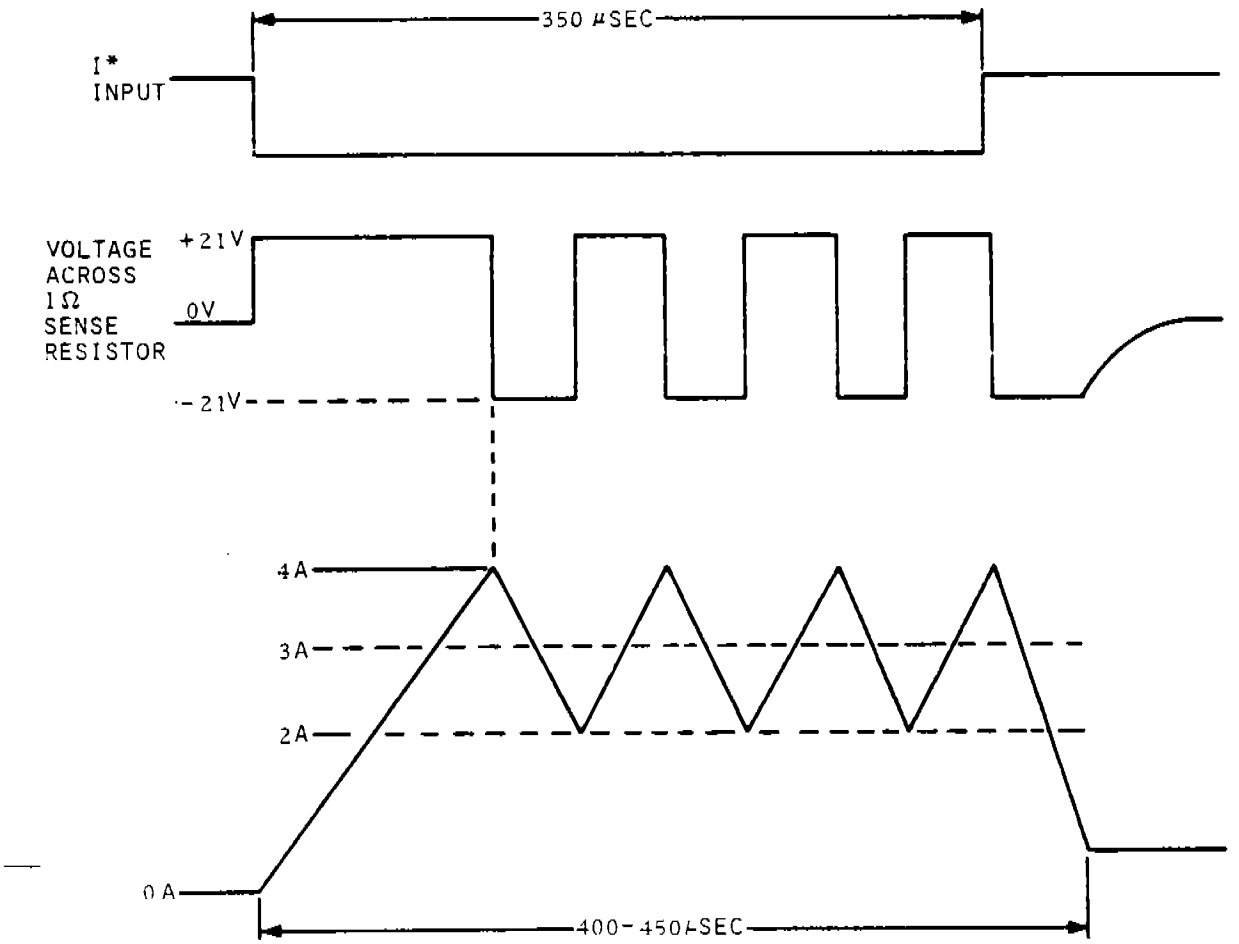



Figure 2-39. Wire Driver Current Waveform

At the point that the 7400 output changes state, the output of OR gate 75463 goes high and turns off power transistors TIP126 and TIP121. The 2 N2222 transistor is immediately turned off, since no more current is flowing through the 1 -ohm resistors; and then the 4700 pF capacitor begins to charge through the internal pull up resistor of NAND gate 7400. When the output of 7400 changes to the low state, the power circuit is again reactivated and begins to build up current in the coil. This "chopping" action continues as long as the input signal is low.

To inhibit the complete circuit from firing, the PS* signal on the input of NAND gate 7400 must go low.

The current control circuit (figure 2-40) controls the reference point on the emitter of every 2N2222 transistor. The 500-ohm potentiometer is used in a voltage divider circuit, dividing the 5.6V reference voltage caused by the 680 - ohm resistor and the IN5232B zener diode. The potentiometer controls the transistor base voltage, which controls the current reference voltage across the TIP126 transistor. The 10-microfarad capacitor is used to filter out any transients.

## 2.8 POWER SUPPLY SYSTEM

The power supply system is composed of two sections: the AC-to-filtered DC converter, and the voltage regulator. The AC-to-filtered DC converter is available in the standard and optional universal versions. The voltage regulator is common to both versions.

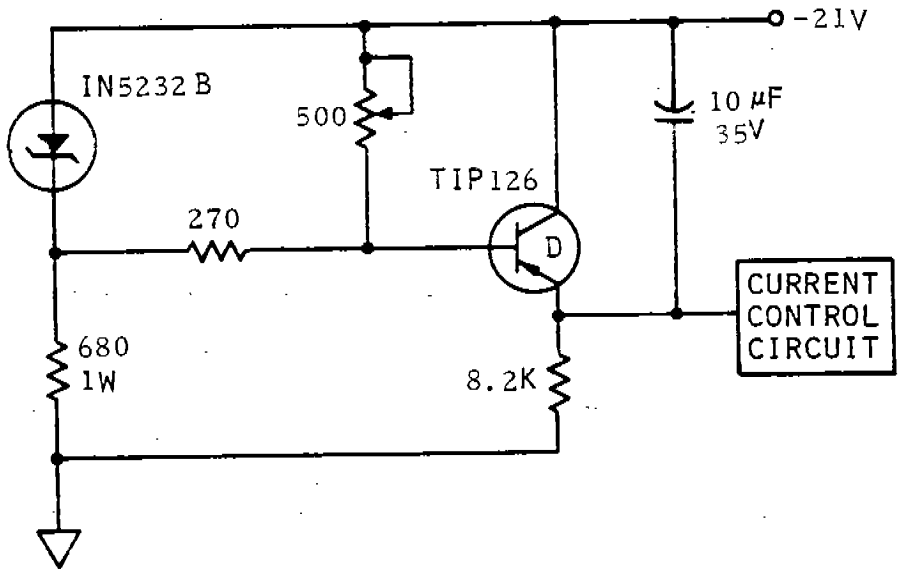
The power supply system is protected against high frequency line noise and switching transients by a line filter which is installed to include suppression of switching transients generated by the POWER ON switch. In the event of excess internal temperatures, a thermosensor will interrupt the AC input power until the temperature drops to its normal operating value. The thermosensor is mounted on the rectifier heat sink assembly located above the transformer.

### 2.8.1 Universal AC-to-Filtered DC Converter

Table 2-18 lists the available input voltages and frequencies which can be programmed into the power supply by simply rearranging the wiring of the program connector TB2 (see figure 2-41). No tools are required to perform the wiring changes.

**TABLE 2-18. UNIVERSAL SUPPLY INPUT VOLTAGES AND FREQUENCIES**

| Nominal Input Voltage | Low Input Voltage | High Input Voltage | Input Freq. Range |
|---|---|---|---|
| 115 VAC | 90 VAC | 127 VAC | 59 to 60.6 HERTZ |
| 250 VAC | 204 VAC | 264 VAC | 59 to 60.6 HERTZ |
| 115 VAC | 90 VAC | 140 VAC | 49 to 50.5 HERTZ |
| 250 VAC | 187 VAC | 264 VAC | 49 to 50.5 HERTZ |




ALL RESISTOR VALUES IN OHMS

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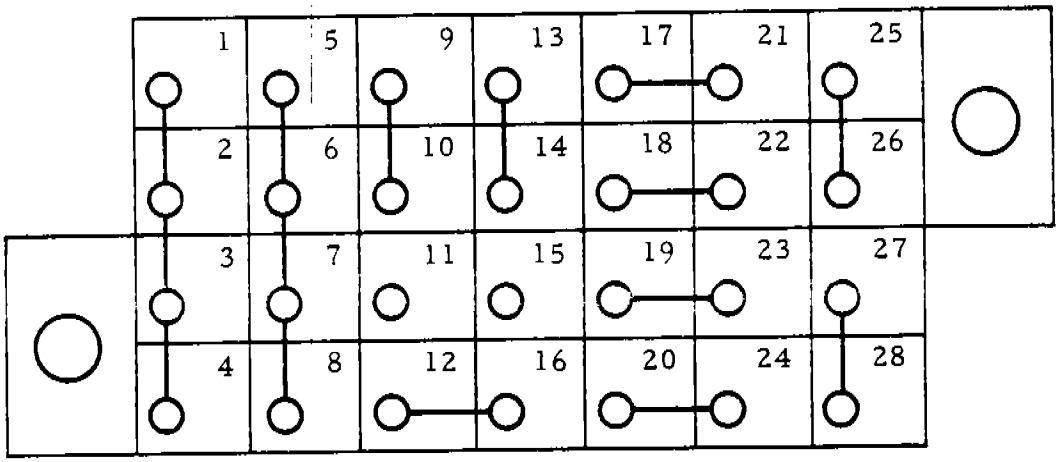
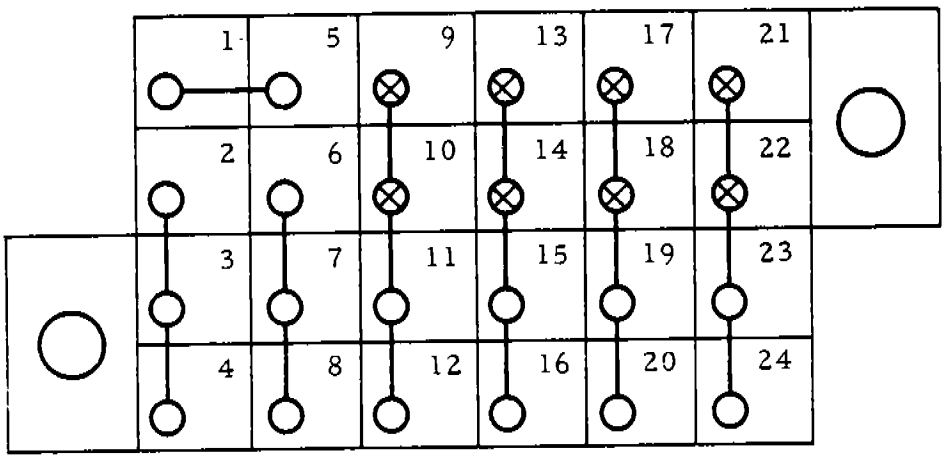
Figure 2-40. Current Control Circuit




TB2




TB1

NOTES

1. PINS MARKED ⊗ HAVE WIRES ON BOTH SIDES.
2. TB1 IS LOCATED ON THE HEATSINK ABOVE TRANSFORMER.
3. TB2 IS LOCATED NEXT TO C4.
4. TB1 AND TB2 VIEWS SHOWN FROM FRONT OF PRINTER.

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Figure 2-41. Terminal Block Pin Configuration

Table 2-19 is the TB2 wire configuration table listing pin position numbers, frequencies, and wire colors.

NOTE

To reconfigure the universal power supply from one power option to another, wires on TB2, C4, and the base terminals must be relocated. Note that the listed color-coded wires shown in table 2-19 may be connected at any one of the several possible locations.

**TABLE 2-19. UNIVERSAL POWER SUPPLY TB2, C4 AND BASE TERMINAL WIRE CONFIGURATION**

| Wire Color | TB2 Pin Position Number | | | |
|---|---|---|---|---|
| | 115 VAC 60 Hz | 115 VAC 50 Hz | 250 VAC 60 Hz | 250 VAC 50 Hz |
| Red** | 8 | 8 | 16 | 16 |
| Orange/Yellow | 6 | 10 | 6 | 10 |
| Orange/White | 9 | 6 | 9 | 6 |
| Brown | 3 | 3 | 7 | 7 |
| Brown/Yellow | 7 | 14 | 12 | 14 |
| Brown/White | 13 | 7 | 13 | 12 |
| White/Orange** | 27 | 26 | 27 | 26 |
| White** | 23 | 24 | 23 | 24 |
| Violet/White** | 22 | 21 | 22 | 21 |
| *Red/White | Base Term | C4 | Base Term | C4 |
| *Red/Black | C4 | Base Term | C4 | Base Term |

* Wires not located on TB2.
**Part of wire harness. In a two-color wire, the first color named is the base color, and the second the color of the stripe.

**NOTE**

For 250V, 50 Hz or 60 Hz operation, replace fuse F1 with a 1.5A, slo-blo. For 115V, 50 Hz or 60 Hz operation, replace fuse F1 with a 3A slo-blo.

2.8.2 Typical Output

Table 2-20 lists typical outputs for the Universal AC-to-filtered DC converter.

**TABLE 2-20. TYPICAL OUTPUTS**

| Item | Specification |
|---|---|
| +21 Volts Output | |
| Minimum: | +18.1 Volts |
| Nominal: | +21 Volts |
| Maximum: | +23.1 Volts |
| Ripple (Standby:) | 1500 Millivolts P-P Maximum |
| Ripple (Self test): | 1.8 Volts P-P Maximum |
| Current (Standby): | 0.5 Amps |
| Current (Self test): | 3.0 Amps |
| -21 Volts Output | |
| Minimum: | -18.9 Volts |
| Nominal: | -21 Volts |
| Maximum: | -23.1 Volts |
| Ripple (Standby): | 250 Millivolts P-P Maximum |
| Ripple (Selftest): | 1.8 Volts P-P Maximum |
| Current (Standby): | 1.5 Amps |
| Current (Self test): | 4.0 Amps |
| +9 Volts Output | |
| Minimum: | +8.1 Volts |
| Nominal: | +9 Volts |
| Maximum: | +9.9 Volts |
| Ripple (Standby): | 300 Millivolts P-P Maximum |
| Ripple (Self test): | 400 Millivolts P-P Maximum |
| Current (Standby): | 2.4 Amps |
| Current (Self test): | 2.4 Amps |
| Input Power | |
| Standby: | 130 Watts |
| Self Test: | 220 Watts |

TABLE 2-20. TYPICAL OUTPUTS (Contd)

| Item | Specification |
|---|---|
| Power On Surge: | Approximately 1000 Volt-Amp for a period of 125 milliseconds, with an applied input voltage of 115 VAC rms. |
| Ambient Operating Temp. | 10°C to 40°C |
| Thermosensor Rating | Normally closed. Opens at heat sink temperature of 75°C and closes at 55°C. |

### 2.8.3 Voltage Regulator CCA Operation

The voltage regulator accepts the unregulated voltages from the AC-to-filtered DC converter and regulates these voltages to the required printer operating voltages. There are three different voltage regulator circuits incorporated in the Voltage Regulator CCA: +12V, -12V, and +5V.

The +12V voltage regulator circuit is comprised of voltage regulator U3, SCR Q5, Zener diode CR3, and associated circuits. U3 is a self-contained integrated circuit, using unregulated +21V to develop the +12V regulated power. Capacitors C11 and C12 prevent high frequency oscillation, while diodes CR4 and CR5 protect against reverse voltage transients. SCR Q5 is a crowbar device that protects the +12V regulator circuit against overload conditions; when load current exceeds the allowable maximum, the increased voltage drop developed across R10 (voltage across CR3 is constant) trips Q5, shorting +12V to ground. Additional overload protection is supplied by F3.

The -12V voltage regulator operates in a manner identical to the +12V regulator. U2 is a negative equivalent of U3, using unregulated -21V to develop the -12V regulated power.

The main component of the +5V regulator circuit is Darlington transistor Q1. Placed in series between the +9V unregulated supply and the +5V load, Q1 acts as a variable impedance, allowing more or less current to flow as dictated by load demands. Integrated circuit U1 acts as a thermo-stable error amplifier. Using the +12V regulated voltage as a reference, U1 supplies an output to the base of Q1. Another input to U1 is the +5V SENSE sample obtained from the Mother Board CCA. This +5V SENSE input has the same characteristics as the +5V regulated output, and affects the output of U1 in an inverse proportion. For example, when the +5V output drops due to an increase in the load, the output of U1 at pin 4 goes more positive, allowing more current to flow through Q1, and returning the +5V output to its regulated value. Conversely, a load decrease tends to drive the +5V output more positive, causing the output of U1 to go more negative. This results in a decreased current flow through Q1.

Transistor Q2 serves as a current limiter to Q1; excessive current through Q1 increases the voltage drop across R3-R4, causing Q2 to conduct more, and resulting in a decreased current flow through Q1. SCR A3 is a crowbar device identical to Q4 and Q5. Additional overload protection in the +5V regulator circuit is provided by fuse F1.

### 2.8.4 Voltage Regulator Output

Table 2-21 lists the voltage regulator output.

**TABLE 2-21. VOLTAGE REGULATOR OUTPUT**

| Parameter | Conditions | Min. | Max. |
|---|---|---|---|
| Positive 5 Volt Output | $I_L \leq 5$ Amp | 4.95 | 5.05 |
| Positive 12 Volt Output | $I_L \leq 300$ mA | 11.4 | 12.6 |
| Negative 12 Volt Output | $I_L \leq -300$ mA | -11.4 | -12.6 |
| $\pm$12 Volt Ripple | $I_L \leq \pm 300$ mA | | $10 \times 10^{-3}$ |
| Positive 5 Volt Over Ripple | $I_L \leq \pm 5$ Amp | | |
| Positive 12 Volt Over Voltage Trip | | 13.5 | 16.5 |
| Negative 12 Volt Over Voltage Trip | | -13.5 | -16.5 |
| Positive 5 Volt Over Voltage | | 6.3 | 7.7 |

## 2.9 TCVFU CCA

The optional TCVFU CCA controls the operation of the TCVFU motor in accordance with signals supplied to it by the Interface CCA and TCVFU tape reader. The TCVFU motor is connected to pins 2 and 1 of J17. Pin 2 of J17, labelled MOTOR+), is connected directly to the +9V supply. Pin 1 of J17, labelled MOTOR-, is connected to the collector junction of Q3. When Q3 is conducting, 9V RTN is connected to the collector junction of Q3, and the TCVFU motor is running. When Q3 is cut off, the TCVFU motor is switched off. Normally, Q3 is cut off and the TCVFU motor is not running.

Action starts when the operator presses the READ switch on the TCVFU tape reader, activating signal TRRQSW* on J1-12. An amplified version of TRRQSW*, signal TRRQ*, is routed through J16-20 to the Interface CCA and ultimately to the Processor CCA. The Processor CCA responds by activating read

enable signal ENRDR*. This signal is routed through the interface CCA to J1-15 of the TCVFU CCA, turning on Q2. With Q2 conducting, W3 is turned on, switching on the TCVFU motor. While Q2 is conducting, +5V LED SUPPLY is provided to the tape reader.

While ENRDR* is active, the sprocket hole in the tape is periodically sensed by the TCVFU reader, activating signal CH13 on J1-28 on the TCVFU CCA. With CH13 active, one-shot U1 is triggered on, momentarily turning on Q1. With Q1 conducting, Q3 is cut off, turning off the TCVFU motor. When U1 times out, the TCVFU motor is turned on once again. Thus, during the on-period of U1 (approximately 190 microseconds) the tape is stopped long enough to allow the TCVFU reader to sense the tape channel positions associated with a given sprocket hole.

# SECTION III

# TROUBLESHOOTING

## 3.1 INTRODUCTION

This section contains information necessary to troubleshoot the printer. Troubleshooting is organized at two levels: the printer system level, and the power distribution level. Information provided in this section is applicable to both M120 and M200 printer models.

## 3.2 PRINTER SYSTEM TROUBLESHOOTING

The printer system troubleshooting guide, table 3-1, lists the status display indicators, their definitions, probable causes and remedies. For assistance in circuit board isolation or assembly troubleshooting, refer to table 3-2, the Fault Probability Guide.

### 3.2.1 System Fault Analysis

This paragraph provides a description of the status codes listed in table 3-1 and an explanation of the way in which each is evolved. Some of the status displays are not error conditions but merely indicate which print system routine is being performed or was being performed when a fault condition occurred.

Fault isolation involving the Interface CCA assumes that the printer is configured with a standard DPC Short-Line Parallel Interface CCA. If the printer is configured with any of the optional Interface CCAs, refer to the applicable logic diagram in Section IV, Volume II of this manual to find the equivalent logic circuit and pin connections.

a. Switch Check Routine/Ready - Status Display 00

This routine monitors the control panel switches and various fault condition switches, which include the following:

1. Form Length Switch
2. On Line Switch
3. Top of Form Switch
4. Paper Step Switch
5. Vertical Pitch Switch
6. Alarm/Clear Switch
7. Bail Open Switch
8. Cover Open Switch (Optional)
9. TCVFU Switch (Optional)

b. Out of Paper - Status Display 01

The paper low interlock switch S5 provides a means of detecting when the printer runs out of paper. When paper is installed in the printer, this switch is held in an energized position. The loss of paper from in front of this

# TABLE 3-1. PRINTER SYSTEM TROUBLESHOOTING GUIDE

| Status Display | Definition | Probable Cause | Remedy |
|---|---|---|---|
| 00 | Switch check routine/ready | Undefined | Replace or repair CCA as required. |
| 01 | Out of paper | No paper | Install paper. |
| 03 | Cover open | Cover not closed or switch defective | Close cover or adjust or replace switch. |
| 04 | Bail open | Platen lever open or switch defective | Close platen gap lever or adjust or replace switch. |
| 09 | No tape - tape reader jammed | No tape, broken tape or jammed tape during tape TCVFU operation | Install tape, correct jam condition. |
| 10 | TCFVU Read/Compare | Unable to read and verify tape successfully | Validate tape. |
| 12 | No TOP OF FORM on tape | No channel 1 hole punched in tape | Install valid tape. |
| 13 | Channel not found | Tape too long | Limit tape to a maximum of 254 lines. |
| 20 | No Character Generator | Character Generator ROM not installed | Install character generator ROM. |
| 26 | DAVFU fault | Stop code after ODD number of bytes, too many data bytes, parity error | Send stop code after even data byte, limit data bytes to 255 or less, validate input data. |
| 40 | Print right normal | Undefined | Replace or repair CCA as required. |
| 41 | Print left normal | | |
| 42 | Print right compressed | | |
| 43 | Print left compressed | | |
| 44 | Print right expanded | | |
| 45 | Print left expanded | | |
| 48 | TCFVU load routine | | |
| 50 | Position seek | | |
| 52 | Shuttle park | | |
| 54 | Initialization routine | | |
| 55 | Form feed routine | | |
| 56 | 6 Lines Per Inch routine | | |
| 57 | 8 Lines Per Inch routine | | |
| 58 | Step routine | | |
| 62 | Buffer not full | Load operation not completed within allowed time | Restart load operation. |
| 63 | Buffer interrogate | Undefined | Replace or repair CCA as required. |
| 64 | No shuttle motion | No shuttle motion within specified time | Mechanical interference, broken belt, defective motor. |
| 65 | No interface card | Interface card not inserted | Install correct interface card. |
| 66 | No clear to alarm C/R flip-flop | Clear F/F failed to reset | Replace or repair Processor CCA. |
| 67 | Self Test | Self test switch in test position | Place self test switch to OFF position. |
| 68 | Shuttle pitch and format switch do not compare | Shuttle pitch is wrong for line of data | Replace or repair Processor CCA |
| 69 | Character column counter incorrect - mechanical failure | Shuttle has passed the point where printing should begin | Replace or repair Processor CCA: repair mechanical problem. |
| 70 | Self Test with I/F | Denotes Self Test routine is being performed with I/F card installed | |

# TABLE 3-2. FAULT PROBABILITY GUIDE

| Malfunction Symptom | Probable Cause | Maintenance Action |
|---|---|---|
| Print density not uniform. | a. Wire Driver ON/OFF period misadjusted. | Adjust. |
| | b. Forms thickness setting does not match form. | Change forms thickness control setting to match form. |
| | c. Wire Driver current misadjusted. | Adjust. |
| | d. Wire Driver CCA A5 defective. | Replace Wire Driver CCA A5. |
| | e. Processor CCA A3 defective. | Replace Processor CCA A3. |
| Print line is skewed. | Tractor phasing incorrect. | Correct tractor phasing. |
| Print rate too slow. | a. Shuttle speed on Motor Driver CCA A4 misadjusted. | Adjust shuttle speed. |
| | b. Excessive shuttle friction. | Clean guide bar with isopropyl or denatured alcohol, or Loctite safety solvent. |
| Random print errors or printer does not respond to user system input. | a. Interface cable not connected properly. | Ensure proper interface cable connection. |
| | b. Interface cable defective. | Replace interface cable. |
| | c. Defective Interface CCA A2. | Replace Interface CCA A2. |
| | d. Serial Interface CCA only: interface parameter switches incorrectly set. | Set interface parameter switches. |
| | e. Processor CCA A3 defective. | Replace Processor CCA A3. |
| Dots missing from printer character. | a. Worn ribbon. | Replace ribbon cartridge. |
| | b. Forms thickness control setting does not match forms thickness. | Place forms thickness control to proper setting. |
| | c. Wire driver ON/OFF period misadjusted. | Adjust |
| | d. Any one of fuses A4F1 through A5F1 on Wire Driver CCA defective. | Replace defective fuse. |
| | e. Wire Driver CCA A5 defective. | Replace Wire Driver CCA A5. |
| | f. Print head defective. | Replace print head. |
| | g. Processor CCA A3 defective. | Replace Processor CCA A3. |
| | h. Defective print head flex cable. | Replace print head flex cable assembly (W3). |
| Margin alignment inconsistent or non-uniform. | a. Loose shuttle servo belt. | Tighten shuttle servo belt. |
| | b. Loose pulley on shuttle servo motor. | Tighten pulley with Allen head wrench. |
| | c. Column 1 harness loose. | Adjust column 1 harness. |
| | d. Flange on carriage loose. | Tighten flange. |
| | e. Forms thickness control does not match form thickness. | Place forms thickness control to correct setting. |
| | f. Processor CCA A3 defective. | Replace CCA A3. |
| | g. Defective shuttle servo motor. | Replace shuttle servo motor. |
| Print head overshoots left or right margin. | a. Column 1 harness misadjusted. | Readjust column 1 harness. |
| | b. A4F3 fuse defective (right overshoot). | Replace A4F3. |
| | c. A4F4 fuse defective (left overshoot). | Replace A4F4. |
| | d. Column 1 harness defective. | Replace column 1 harness. |
| | e. -21 volt power absent (left overshoot). | |
| | f. +21 volt power absent (right overshoot). | |
| | g. Shuttle servo motor defective. | Replace shuttle servo motor. |
| | h. Motor Driver CCA A4 defective. | Replace Motor Driver CCA A4. |
| | i. Processor CCA A3 defective. | Replace Processor CCA A3. |

## TABLE 3-2. FAULT PROBABILITY GUIDE (Contd)

| Malfunction Symptom | Probable Cause | Maintenance Action |
|---|---|---|
| Paper does not advance when the PAPER STEP switch is pressed. | Printer is in the on line mode?<br>NO<br>YES | Press the ON LINE switch to go off line. |
| | J10-31 on the control panel goes low when the PAPER STEP switch is pressed?<br>NO<br>YES | PAPER STEP switch defective. Replace control panel assembly. |
| | P2-46 Processor CCA connector goes low when the PAPER STEP switch is pressed?<br>NO<br>YES | Defective cable connection from the Control Panel PAPER STEP switch to the Processor CCA. Repair or replace as necessary. |
| | U31-16 on the Processor CCA goes low when the PAPER STEP switch is pressed?<br>NO<br>YES | Defective I.C. U31. |
| | U22-18 on the Processor CCA is low during the positive-going edge of the clock pulse?<br>NO<br>YES | Defective circuitry on the Processor CCA. Repair or replace Processor CCA. |
| | P1-17 on the Processor CCA (STEP*) goes low after pressing the PAPER STEP switch?<br>NO<br>YES | Defective I.C. U22 or connection. |
| | U8-6 on the Motor Driver CCA (STEP*) goes low after pressing the PAPER STEP switch?<br>NO<br>YES | Defective connection from Motor Driver CCA to the Processor CCA. |
| | U8-4 on the Motor Driver CCA goes high after pressing the PAPER STEP switch?<br>NO<br>YES | Defective I.C. U8 or associated circuitry. |
| | P1-47 on the Motor Driver CCA goes to approximately +21V after pressing the PAPER STEP switch?<br>NO<br>YES | Defective F1, Q11, Q12, or associated circuitry, or +21V supply voltage. |
| | P1-18 on the Motor Driver CCA (Phase 1) goes low after initial power on?<br>YES | Defective connection from the Motor Driver CCA to the Processor CCA, or the Processor CCA defective. |

## TABLE 3-2. FAULT PROBABILITY GUIDE (Contd)

| Malfunction System | Probable Cause | Maintenance Action |
|---|---|---|
| When PAPER STEP switch is pressed and released, paper advances continuously. | a. PAPER STEP switch defective.<br>b. Motor Driver CCA A4 defective.<br>c. Processor CCA A3 defective. | Replace control panel assembly.<br>Replace Motor Driver CCA A4.<br>Replace Processor CCA A3. |
| Paper does not align to top of form position. | a. Paper improperly loaded.<br>b. 6/8 LPI switch option improperly set.<br>c. FORM LENGTH switch option improperly set.<br>d. Paper feed belt broken.<br>e. TCVFU improperly loaded.<br>f. Tape reader defective.<br>g. VFU tape defective. | Reload paper.<br>Verify that 6/8 LPI switch is set to correct position.<br>Verify that FORM LENGTH switch setting agrees with forms being used.<br>Replace paper feed belt.<br>Reload TCVFU.<br>Replace tape reader.<br>Replace VFU tape. |
| ON LINE indicator does not go on after ON LINE switch is pressed; ALARM indicator is on. | a. Printer is out of paper.<br>b. Paper low interlock switch misaligned.<br>c. Platen gap lever in open position, or bail open interlock switch misadjusted or defective.<br>d. Processor CCA defective. | Load paper.<br>Adjust.<br>Close platen gap lever, adjust bail open interlock switch, or replace if defective.<br>Replace Processor CCA A3. |
| Printer continues printing after paper supply has been exhausted. | Paper low interlock switch misadjusted or defective. | Replace or adjust low interlock switch as appropriate. |
| Ribbon is not advancing. | Ribbon cassette improperly installed or defective?<br>NO<br>YES | Install or replace as needed. |
| | P1-5 on the Motor Driver CCA at +21V?<br>NO<br>YES | Fuse A4F1 open or +21V supply missing. Replace fuse or repair power supply as needed. |
| | P1-20 on the Processor CCA (RMTR*) goes low on a print or form feed operation?<br>NO<br>YES | Defective Processor CCA A3. Replace |
| | P1-20 on the Motor Driver CCA (RM*) goes low on a print or form feed operation?<br>NO<br>YES | Defective connection between Processor CCA and the Motor Driver CCA A4. Repair. |
| | U13-6 on the Motor Driver CCA goes high on a print or form feed operation?<br>NO<br>YES | Defective I.C. U13 or associated circuitry. Replace I.C. or repair circuitry as necessary. |

## TABLE 3-2. FAULT PROBABILITY GUIDE (Contd)

| Malfunction Symptom | Probable Cause | Maintenance Action |
|---|---|---|
| Ribbon is not advancing. (Contd) | P1-7 on the Motor Driver CCA (RMNEG) goes low on a print or form feed operation?<br>NO<br>YES | <br>Defective Q14. Replace.<br>Defective Ribbon Motor. Replace. |
| Carriage does not move or moves erratically. | a. Mechanical interference such as paper jam.<br>b. Idler pulley misadjusted.<br>c. Push-on terminals to shuttle servo motor disconnected.<br>d. Shuttle servo belt broken.<br>e. Fuse A4F3 and/or A4F4 on Motor Driver CCA A4 defective.<br>f. Power supply voltage absent.<br>g. Motor Driver CCA A4 defective.<br>h. Processor CCA A3 defective. | Remove cause of interference.<br>Adjust idler pulley adjustment knob.<br>Connect terminals to shuttle servo motor.<br><br>Replace<br>Replace fuse(s)<br><br>Replace Motor Driver CCA A4.<br>Replace Processor CCA A3. |
| Printer does not operate when power switch is turned on. | a. Printer power cord not connected to power source.<br>b. Primary power fuse F1 defective.<br>c. Power switch S1 defective. | Connect power cord to power source<br>Replace F1.<br>Replace S1. |
| ON LINE indicator does not go on after the ON LINE switch has been pressed; ALARM indicator is off. | J10-12 on Control Panel (ON LINE LMP)* is low?<br>NO<br><br>YES | <br><br>ON/LINE indicator defective or +20V supply to indicator lamp is missing. Replace lamp or check power supply. |
| | P1-44 on the Processor CCA (ON LINE LMP*) is low?<br>NO<br><br>YES | <br><br>Defective connection between Processor CCA and Control Panel. Repair. |
| | U35-6 on the Processor CCA (ON LINE LMP*) is low?<br>NO<br>YES | <br><br>I.C. U35 defective. Replace. |
| | J10 -33 on the Control Panel (ON/OFF LINE*) goes low when the ON LINE switch is pressed?<br>NO<br>YES | <br><br><br>Defective switch assembly. Replace. |
| | P2-47 on the Processor CCA (ON/OFF LINE*) goes low when the ON LINE switch is pressed?<br>NO<br><br>YES | <br><br><br>Defective connection between the Processor CCA and Control Panel. Repair. |
| | U12-5 on the Processor CCA (ON LINE FLOP) is high?<br>NO<br><br>YES | <br><br>I.C. U12 or associated circuitry defective. Replace.<br>Processor CCA A3 defective. Replace. |

## TABLE 3-2. FAULT PROBABILITY GUIDE (Contd)

| Malfunction Symptom | Probable Cause | Maintenance Action |
|---|---|---|
| Paper does not advance under any condition. | Paper feed belt broken?<br>NO<br>YES | Replace paper feed belt. |
| | Tractor drive assembly binding or defective?<br>NO<br>YES | Repair or replace tractor drive assembly as needed. |
| | P1-17 on the Motor Driver CCA (STEP*) goes low on a paper move command or when pressing the PAPER STEP switch or TOP OF FORM switch?<br>NO<br>YES | Defective Processor CCA A3 or bad connection from the Processor CCA A3 to the Motor Driver CCA A4. Repair or replace as needed. |
| | P1-47 on the Motor Driver CCA (STEP*) goes to approximately +21V on a paper move command or when pressing the PAPER STEP switch or TOP OF FORM switch?<br>NO<br>YES | Fuse A4F1 open, +21V supply missing, or defective circuitry on the Motor Driver CCA A4. Repair or replace as needed. |
| | P1-18 on the Motor Driver CCA (01*) goes low on initial power on?<br>NO<br>YES | Defective Processor CCA A3 or bad connection from the Processor CCA to the Motor Driver CCA A4. Repair or replace as needed. |
| | P1-43 on the Motor Driver CCA (PM01) is at approximately -21V?<br>NO<br>YES | Fuse A4F2 open, -27V supply missing, or defective circuitry on the Motor Driver CCA A4. Repair or replace as needed.<br>Replace the paper step motor. |

## TABLE 3-2. FAULT PROBABILITY GUIDE (Contd)

| Malfunction Symptom | Probable Cause | Maintenance Action |
|---|---|---|
| Paper does not advance when the PAPER STEP switch is pressed. | U8-10 on the Motor Driver CCA is high?<br>NO<br>YES | Defective I.C. U8 |
| | P1-43 on the Motor Driver CCA (PM1) is at approximately -21V?<br>NO<br>YES | Open fuse F2, associated components, or -21V supply voltage.<br>Replace the Paper Feed Step Motor. |
| In self test mode, paper does not advance after each line of print (overprint). | Processor CCA A3 defective. | Replace Processor CCA A3. |
| With printer on line, and interface connected, paper advances incorrect number of lines. | a. Interface CCA A2 defective.<br>b. Processor CCA A3 defective. | Replace Processor CCA A2.<br>Replace CCA A3 |
| Paper does not advance when TOP OF FORM switch is pressed. | Printer is in the on line mode?<br>NO<br>YES | Press ON LINE switch to go off line. |
| | J10-30 on the control panel goes low when the TOP OF FORM switch is pressed?<br>NO<br>YES | TOP OF FORM switch defective. Replace control panel assembly. |
| | P2-42 on Processor CCA connector goes low when TOP OF FORM switch is pressed?<br>NO<br>YES | Defective cable connection from the control panel TOP OF FORM switch to the Processor CCA.<br>Defective Processor CCA. Replace |

switch allows the switch contact to open, thereby supplying a high level at connector P2-41 of the Processor CCA (see Section IV, Volume II). This high input is provided to input port driver U31-11. When U31-1 is enabled, U31-9 is then set, gating DBUS5 through I/O port transceiver U27 to system controller U19 and Processor Chip U2.

Under program control, the data bits are examined and determined to be in a paper low condition. The shuttle is parked if it has been moving, and the ribbon drive motor and the ON LINE indicator are turned off. The ALARM indicator is turned on, and the system data bus lines from bi-directional driver U20 on the Processor CCA are sent to the status display indicators where a status code of 01 is displayed.

Installation of paper and pressing the ALARM/CLEAR switch will restore the printer to normal operation.

c. Cover Open - Status Display 03

An optional cover open switch is provided on the printer. If the printer cover is opened while printing, the printer will go to an off-line condition, and the print head will be parked at the end of the present print cycle.

With the cover closed, the cover open switch is held in an energized position. Opening the cover allows its contacts to close, supplying a low level at connector P2-43 of the Processor CCA (see Section IV, Volume II). This low level is placed on input port driver U31-13. When U31-1 is enabled, U31-7 is set, gating DBUS6 low through I/O port transceiver U29 to system controller U19 and Processor Chip U2.

Under program control, the data bits are tested and found to be in a cover-open condition. The shuttle is parked, and the ribbon driver motor and ON LINE indicator are turned off. Pressing the ON LINE switch while the cover is open will light the ALARM indicator. The system data bus lines from the bi-directional driver U28 on the Processor CCA are then sent to the status display indicators on the control panel, where a status code of 03 will be displayed.

Closing the cover and pressing the CLEAR switch will clear the fault condition and restore the printer to normal operation.

d. Bail Open - Status Display 04

The platen gap lever, if left open or if opened during printer operation, will take the printer off line and prevent printer operation due to a bail open condition. With the platen closed, the bail switch is in a de-energized position. Opening the platen supplies a high level at connector P2-45 of the Processor CCA (see Section IV, Volume II). This high level is placed on input port driver U31-2. When U31-1 is enabled, U31-18 (data Bus 4) is gated to the I/O port transceiver U27 system controller and processor chip U2.

Under program control, the data bits are tested and found to be in a bail-open condition. If the printer is powered up with the bail open, the ALARM light will be lit and status code of 04 will be displayed. If the bail is opened while

the printer is operating, the shuttle is parked, and the ribbon drive motor and ON LINE indicator are turned off. Pressing the ON LINE switch with the bail open will turn on the ALARM light and gate the system data bus lines from bi-directional driver U28 on the Processor CCA to the status display indicators. A status code of 04 will then be displayed.

Closing the bail and pressing the CLEAR switch will clear the fault condition and restore the printer to normal operation.

e. No Tape - Tape Reader Jam -Status Display 09

One of the options available to the printer system is the tape controlled vertical format unit (TCVFU). This option sets up the correct format control for the printer.

When a TCVFU load operation is desired, the printer must be in the off line mode, and the switch located on the tape reader unit must be manually pressed. Pressing the tape reader switch develops the signal TRRQ (Tape Reader Request) on the Interface CCA (See Section IV, Volume II). Signal TRRQ on J12-20 is routed through the lower tape channel port and through the first interface port of the applicable Interface CCA to interface data bus DBUF1-DBUF8. Under program control, the Processor CCA examines the contents of DBUF1-DBUF8, detects the presence of TRRQ, and determines that it is a call for a TCVFU load routine. Movement of the tape reader develops a tape reader strobe pulse. This strobe pulse is developed from the tape sprocket feed holes and arrives at connector J12-28 on the Interface CCA as signal CH13 (Tape Channel 13). The input is sent to U19-17, and when enabled by CS7* at U19-1, it outputs U19-3 (DBU~8) onto the interface data bus.

Under program control, this data bus is examined, and if no strobe pulse occurs at DBUF8, it is determined that either no tape has been installed, or a tape reader jam has occurred. The TCVFU drive motor then turns off, the ALARM indicator illuminates, and a status code of 09 is displayed.

Correction of the problem that caused the error condition, pressing the CLEAR switch, and repeating the load operation will restore normal printer operation.

f. TCVFU Read/Compare - Status Display 10

If the TCVFU fails to read and compare for two consecutive times during the five read operations allowed, tape operation will halt and a status code of 10 will be displayed.

During the TCVFU load routine, data read from the TCVFU tape is input to the VFU memory. A programmed count of five allows the user to read the tape and compare it with the VFU memory for a maximum of five times. Each time the tape is read and no comparison occurs, the VFU memory is changed to reflect the new data, and the programmed count of five is decremented. If the VFU memory does not match the tape within two consecutive readings and within the five tries allowed, a fault condition has occurred. The TCVFU drive motor will then turn off, the ALARM indicator will be lit, and a status code of 10 will be displayed.

Correction of the cause of the error condition, pressing the CLEAR switch, and restarting the tape read operation will restore normal printer operation.

g. No Top of Form - Status Display 12

The TCVFU tape may be punched with any combination of twelve channels, with the exception that channel 1 represents the top of form, and channel 12 represents the bottom of form. During the initial tape read operation, a check is made to ensure that the top of form hole punched in channel 1 is correctly punched in the tape.

The output of channel 1 (CH1) arrives at J12-34 of the applicable Interface CCA (see Section IV, Volume II). The CH1 output from the tape reader goes low when that channel is sensed. If after reading the tape, CH1 has not been sensed, U19-18 will not be activated. Under program control, this sequence will be checked, the TCVFU drive motor will be turned off, the ALARM indicator will be illuminated, and a status code of 12 will be displayed.

Inserting a correctly punched tape, pressing the CLEAR switch, and restarting the tape load operation will restore normal printer operation.

h. Channel Not Found - Status Display 13

Failure to find the Top of Form within 254 lines after it has appeared the first time will cause a status code of 13 to be displayed. After each line of TCVFU data is read, a check is made to determine if a TOF Code, Channel 1, is present. The output of Channel 1 arrives at J12-34 of the applicable Interface CCA (see Section IV, Volume II). Signal CH1 from the tape reader goes low when that channel is sensed. Failure of driver U19-18, the interface data bus line, to be activated before a pre-programmed count of 254 has expired, will inform the printer system that the tape is too long. The TCVFU drive motor will be turned off, the ALARM indicator will be illuminated, and a status code of 13 will be displayed.

Inserting a tape of correct length, pressing the CLEAR switch, and restarting the tape load operation will restore normal printer operation.

i. No Character Generator - Status Display 20

A program check is performed to ascertain whether or not the character generator ROM, MEM5, on the Processor CCA (see Section IV, Volume II) is installed. Under program control, a specified ROM location containing all zeros is read and compared. Failure of the ROM to be installed will bring the ROM output to a high level. Comparison of the specified ROM location when PROM has not been installed will cause a fault condition. Printer operation will stop, the ALARM indicator will be illuminated, and a status code of 20 will be displayed.

Installing a character generator ROM, pressing the CLEAR switch, and restarting the print operation will restore normal printer operation.

j. DAVFU Fault - Status Display 26

The Direct Access Vertical Format Unit (DAVFU) allows format information to be loaded directly from the user system into memory without the need for a tape loop.

In the applicable Interface CCA, DAVFU memory is loaded by sending a start code (156 octal) with the Paper Instruction (P.I.) high. Loading is halted by sending a stop code (157 octal) with the P.I. high.

When loading DAVFU memory, the first data byte received represents tape channels 1 through 6, and the second data byte represents channels 7 through 12. Thus, the data bytes must be loaded in pairs to prevent formatting errors. The maximum number of data byte pairs read into memory is 255, not including start and stop codes.

During the loading of the DAVFU memory, the following errors will be detected: (1) receipt of a stop code after an odd number of data bytes, (2) sending more data bytes than allowed, (3) parity error detection during the loading of DAVFU data.

1. Receipt of a Stop Code After An Odd Number of Data Bytes - When the printer is configured with a DPC Parallel Interface CCA, receipt of a DAVFU stop code with an odd character count (ACBIT1 high) enables NAND gate U11-11, setting DAVFU fault flip-flop U10 (see sheet 7 of DPC Parallel Interface CCA logic diagram in Volume II of this manual). The output of U10, signal DAVFU FAULT*, is channelled through U40 and U57 (sheet 9 of Parallel Interface CCA logic diagram) to bit DBUF3, informing the Processor CCA that DAVFU fault exists.

When the printer is configured with a DPC Centronics-Compatible Interface CCA, receipt of a DAVFU stop code with an odd character count (MEM ADD1 high) enables NAND gate U26-6, setting DAVFU FAULT* flip-flop U25 (see sheet 7 of DPC Centronics-Compatible Interface CCA logic diagram in Volume II of this manual). The output of U25, signal DAVFU FAULT*, is channeled through U38 and U53 (sheet 3 of the DPC Centronics-Compatible logic diagram) to bit DBUF3, informing the Processor CCA that a DAVFU fault exists.

When the printer is configured with a Serial Interface CCA, all DAVFU errors are detected under software control by the processor chip U1 (see sheet 2 of the Serial Interface CCA logic diagram in Volume II of this manual).

2. Sending More Data Bytes Than Allowed - In response to TRRQ, the Processor CCA generates enable signal ENRD* (low, when active). This signal is routed through P2-48 and J12-15 of the applicable Interface CCA to J16-15 of the TCVFU CCA, turning on the tape drive motor.

In printers configured with a Short Line Parallel Interface CCA, a special group of logic circuits monitors the number of DAVFU bytes received from the user. When the number of DAVFU bytes exceeds the maximum allowed (510), a DAVFU FAULT* signal is transmitted by the Interface CCA to the Processor CCA.

Logic circuits implementing this error-detect function are shown in sheet 7 of the Short Line Parallel Interface CCA (see Volume II of this manual). Memory chip MEM3 monitors the accumulated byte count by sampling ACBIT1-ACBIT9. When that count reaches 510, MEM1 generates signal TOP CNT, which is applied to U11-1. Along with TOP CNT, NAND gate U11-3 monitors an inverted version of DA STOP CODE. If TOP CNT is high when DA STOP CODE is still low (top count has been reached but no stop code as yet), on the next byte signal STROBE WRITE clocks flip-flop U10 into the set state, generating signal DAVFU FAULT*.

In printers configured with a DPC Centronics-Compatible Interface CCA, excess DAVFU byte detection is implemented in a manner similar to that of the Short Line Parallel Interface CCA. As shown in sheet 7 of the DPC Centronics-Compatible Interface logic diagram (Volume II of this manual), NAND gate U26-11 monitors both signal 510 and an inverted version of DAVFU STOP. If 510 is high while DAVFU STOP is still low, the next DATA STROBE* signal clocks flip-flop U16 into the set state, generating signal DAVFU FAULT*.

In printers configured with a Short Line Parallel Interface CCA, receipt of a DAVFU byte with a parity error is detected by gate U3-6 (sheet 7 of the Short Line Parallel Interface CCA logic diagram). When gate U3-6 is enabled, it DC-sets flip-flop U10, generating signal DAVFU FAULT*

In printers configured with a DPC Centronics-Compatible Interface CCA, there are no provisions for detecting a parity error.

Pressing the ALARM/CLEAR switch and restarting the load procedure will restore normal printer operation.

k. Print Right Normal - Status Display 40

This routine defines the shuttle servo motor as moving at a right pitch and not in an expanded or compressed print mode. Normal print mode is 10 characters per inch.

l. Print Left Normal - Status Display 41

This routine defines the shuttle servo motor as moving at a left pitch and not in an expanded or compressed print mode. Normal print mode is 10 characters per inch.

m. Print Right Compressed - Status Display 42

This routine defines the shuttle servo motor as moving at a right pitch and in a compressed print mode. Compressed print is 16 characters per inch.

n. Print Left Compressed - Status Display 43

This routine defines the shuttle servo motor as moving at a left pitch and in a compressed print code. Compressed print is 16 characters per inch.

o. Print Right Expanded - Status Display 44

This routine will print from left to right at 5 characters per inch.

p. Print Left Expanded - Status Display 45

This routine will print from right to left at 5 characters per inch.

q. TCVFU Load Routine - Status Display 48

The TCVFU tape is read, and the data is stored in the VFU memory. If the tape read does not compare with the VFU memory within a maximum of five times, a fault condition will occur. A VFU-loaded signal to the user, except in the case of the DPC Centronics-Compatible Interface CCA, will also be set or reset.

r. Position Seek - Status Display 50

This routine is used to position the print head in the quickest way to print a new line.

s. Shuttle Park - Status Display 52

This routine is used to reinitialize the shuttle location with respect to the column one sensor, and also to park the shuttle. The shuttle is parked approximately seven character columns to the right of the sensor.

t. Initialization Routine - Status Display 54

This routine initializes the paper feed motor, various flags, registers and ports; parks the shuttle; checks for an Interface CCA; and shuts off the display indicator lamp.

u. Form Feed Routine - Status Display 55

This routine slews paper the required distance as indicated by the Forms Length Counter (FLC) plus the number of lines required for Perforation Skipover (SKPLNS).

v. Six Lines Per Inch Routine - Status Display 56

This routine moves the paper feed motor through four phases, resulting in the moving of paper one line feed at six lines per inch.

w. Eight Lines Per Inch Routine - Status Display 57

This routine moves the paper feed motor through three phases, resulting in the moving of paper one line feed at eight lines per inch.

x. Step Routine - Status Display 58

This routine moves the paper feed motor one phase. The phase that is on when the routine is entered will be turned off, and the next phase will be turned on.

y. Buffer Not Full - Status Display 62

A LOAD BUFFER signal is sent to the Interface CCA to initiate a load operation. A 30-ms delay is allowed to complete the load operation. If the BUFFER FULL signal, signifying that the load operation is complete does not arrive before the 30 ms load delay times out, the shuttle will be stopped.

Under program control, the system data bus is checked and if signal BUFFER FULL has not arrived within the allotted 30 ms allowed from the start of the load operation, the shuttle will be stopped and a status code of 62 will be displayed.

z. Buffer Interrogate - Status Display 63

This routine is used to interrogate the buffer for terminating code, DAVFU format information, illegal characters, underline codes, and the first and last printable characters.

aa. No Shuttle Motion - Status Display 64

A means of detecting the absence of shuttle motion is provided in the printer system by sensing the encoder pulses. The encoder logic is comprised of two D-type flip-flops, U11-5 and U11-9 on the Processor CCA (see logic diagram in Volume II, sheet 4 of the Processor CCA of this manual). U11-9 will be set when the shuttle is moving to the right, and U11-5 will be set when the shuttle is moving to the left.

A programmed time delay of one second is provided during which time a check is made to see if shuttle motion has occurred.

Encoder flip-flop outputs U11-9 and U11-5 are gated by U36-1 ( ENC INT REQ*) to the 8080 CPU chip as an interrupt, and also to input port U31-15 (sheet 4). When U31-1 is enabled, U31-5 (DBUS7) will be output high or low, depending on the status of the encoder signal U31-15. This output is sent to the Processor CCA, where it is checked under program control. If encoder pulses fail to occur within the allotted time, a fault condition has occurred. The shuttle and ribbon drive motors will be turned off, READY and ON LINE will go low, and a status code of 64 will be displayed.

Pressing the CLEAR switch will reinitialize the printer sy tem.

bb. No Interface CCA - Status Display 65

A means of verifying that the Interface CCA is installed in the printer has been provided. During the power up and initializing procedures, a check is made to verify installation of an Interface CCA. Data of all zeros is written into

location zero of the Interface RAM. This data is then read back. If it compares, the Interface RAM flag is set, denoting that the Interface CCA is in the printer. If the data read back does not compare, the Interface RAM flag is reset to inform the Processor CCA of the absence of the Interface CCA.

If the printer is in the self test mode, the Interface CCA is not needed, and printing will continue. If not in the self test mode, a check of the Interface RAM flag is made, and if it is in the reset condition, printer operation is discontinued, the ALARM indicator is illuminated, and the status code of 65 will be displayed.

Installing an Interface CCA and pressing the CLEAR switch will restore the printer to normal operation.

cc. No Clear to Alarm C/R Flip-Flop - Status Display 66

During power up, a software reset signal is provided to initialize the printer circuitry. A check is then made on the CLEAR flip-flop to be certain that it has been reset. On the Processor CCA (see sheet 4 of the Processor CCA logic diagram in Volume II of this manual), CLEAR flip-flop output U19-9 will be low when in a reset condition. This output is sent to input port driver U21-11 (sheet 4). When U21-1 (CS13*) is enabled, U12-9 (DB5) will be low if the CLEAR flip-flop is reset, or high if the CLEAR flip-flop is not reset. This data is sent to the CPU and Control section of the Processor CCA, where it is checked under program control. If the CLEAR flip-flop is found not to be reset, all motors are turned off, a status code of 66 will be displayed, and printer operation will come to a halt.

Correcting the condition that caused the failure and powering the printer down, and then up, will clear the fault condition.

dd. Self Test - Status Display 67

This routine sets up the self test buffer, generating a fixed pattern printout. One hundred thirty two characters and a line feed are loaded into the buffer. Both status displays are checked by counting from 0 to F. Whether or not an Interface CCA is installed in the printer is also checked. If no Interface CCA is installed, the Processor CCA RAM is selected as the print buffer, starting the printout with a small "a". If the Interface CCA is installed, the Interface CCA RAM is selected as the print buffer, starting the printout with a capital "A".

ee. Shuttle Pitch Wrong for Line of Data - Status Display 68

During the executive routine portion of the program, a comparison of shuttle pitch and horizontal format switch setting is made to be certain that the shuttle is correctly set for the line of data to be printed. If the switch is found to be incorrectly set, the shuttle is parked, a status code of 68 is displayed, and the program is reinitialized.

ff. Shuttle Has Passed Point Where Printing Should Begin-Status Display 69

During the executive routine portion of the program, the direction in which the shuttle is moving is checked, and a check is then made to see if printing is to be normal, compressed, or expanded. The character column counter, which contains the correct character column position of the print head, is then checked to make certain that it is correct for the type of printing to be done. If it is not correct, a status code of 69 will be displayed and the routine will be restarted.

gg. Self Test With Interface - Status Display 70

This display denotes that the self test routine is being performed with the Interface RAM being used as the print buffer. The printout will start off with a capital "A".

## 3.3 POWER DISTRIBUTION

Figure 3-1 is a troubleshooting flow chart of the power supply and other components related to power generation and distribution. Use the power supply schematic diagram in conjunction with figure 3-1 to isolate any faulty power components. Procedures for removing faulty power components are provided in the M120/M200 Maintenance Guide, DPC Part No. 255074.

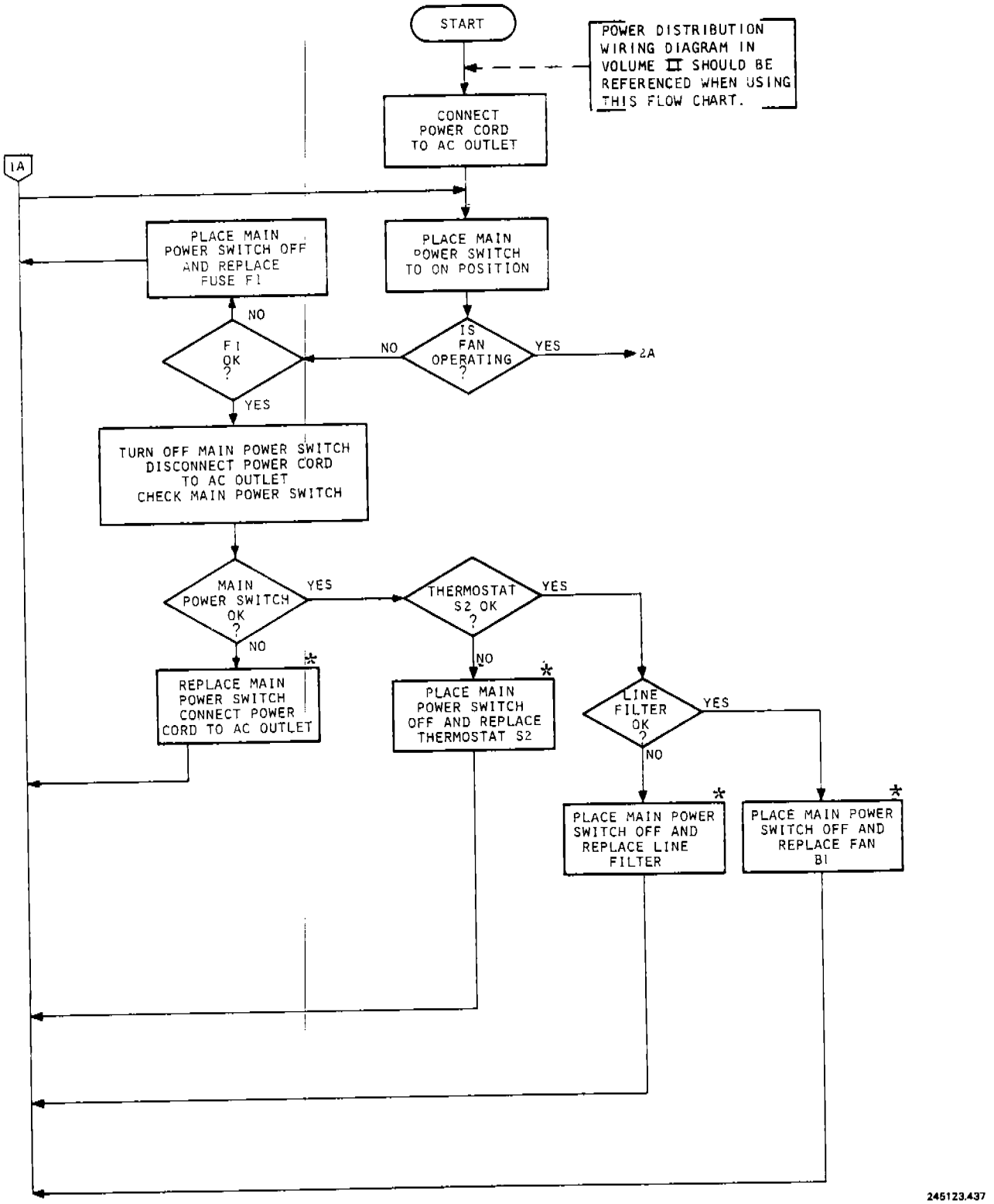


Figure 3-1A. Power Distribution Troubleshooting Flow Chart

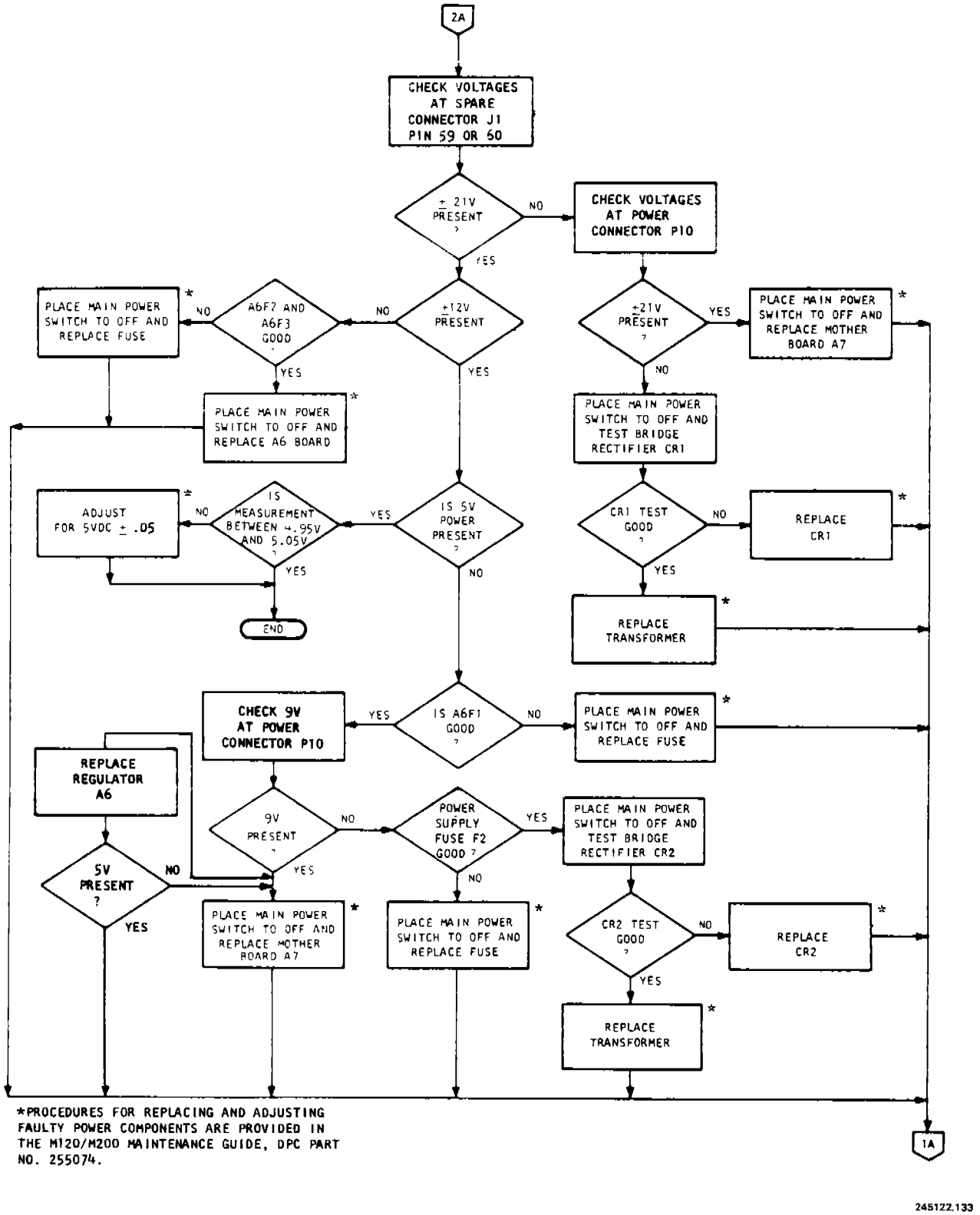


Figure 3-1B. Power Distribution Troubleshooting Flow Chart

# ALPHABETICAL INDEX

## ALPHABETICAL INDEX (Cont'd)

## ALPHABETICAL INDEX (Cont'd)

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